

Appendix E1: IBIS Model Syntax

Roy Leventhal
Used with permission of 3Com

Reference IBIS 3.2

Contents

Table 1: General Rules	9
Format	9
File Names.....	9
Reserved Words	9
POWER.....	9
GND.....	9
NC.....	9
NA.....	9
Line Length	9
Comments.....	9
Keywords	9
Allowed Scaling Factor Prefixes.....	9
Tab characters	9
Temperature	9
Currents	9
Table 2: General Properties	10
[IBIS Ver].....	10
[Comment Char].....	10
[File Name]	10
[File Rev].....	10
[Date].....	10
[Source]	10
[Notes].....	10
[Copyright].....	10
[Disclaimer].....	10
Table 3: Component Properties	12
[Component].....	12
Si_location	12
Timing_location.....	12
[Manufacturer]	12
[Voltage Range]	12
[Temperature Range].....	12
[END]	12
Table 4: Package and Pin Properties	13
[Package].....	13
R_pkg.....	13
L_pkg	13
C_pkg.....	13
[Pin].....	13
signal_name	13
model_name.....	13
R_pin.....	13

L_pin	13
C_pin	13
[Package Model]	15
[Define Package Model]	15
[Manufacturer]	19
[OEM]	19
[Description]	19
[Number of Pins]	19
[Pin Numbers]	19
Len	19
L, R, C	19
Fork	19
Endfork	19
[Number Of Sections]	22
[Model Data]	22
[Resistance Matrix]	23
[Inductance Matrix]	23
Banded_matrix	23
Sparse_matrix	23
Full_matrix	23
[Capacitance Matrix]	27
[Row]	27
[Bandwidth]	27
[End Model Data]	27
[Pin Mapping]	28
pulldown_ref:	28
pullup_ref:	28
gnd_clamp_ref:	28
power_clamp_ref:	28
[Rac]	30
[Cac]	30
[Rgnd]	30
[Rpower]	30
[Diff Pin]	30
inv_pin:	30
vdiff:	30
tdelay_typ:	30
tdelay_min:	30
Tdelay_max:	30
[Series Pin Mapping]	33
pin_2:	33
model_name:	33
funtion_table_group:	33
[Series Switch Groups]	33
On, Off	33
[End Package Model]	33

Table 5: V-I Behavioral Properties.....	36
[Model].....	36
Model_type.....	36
C_comp: Note 1*.....	36
Polarity.....	36
Enable.....	36
Vinl.....	36
Vinh.....	36
[On].....	39
[Off].....	39
[R Series].....	39
[L Series].....	39
[C Series].....	39
[Rl Series].....	39
[Rc Series].....	39
[Lc Series].....	39
[Series Current].....	39
[Series MOSFET].....	39
Vds.....	39
Vol, Voh.....	44
Technology.....	44
[Pulldown].....	44
[Pullup].....	44
[GND Clamp].....	44
[POWER Clamp].....	44
[Pullup Reference].....	48
[Pulldown Reference].....	48
[GND Clamp Reference].....	48
[POWER Clamp Reference].....	48
[Model Selector].....	49
[Model Spec].....	51
Vinh.....	51
Vinh+.....	51
Vinh-.....	51
Vinl+.....	51
Vinl-.....	51
S_overshoot_high.....	51
S_overshoot_low.....	51
D_overshoot_high.....	51
D_overshoot_low.....	51
D_overshoot_time.....	51
Pulse_high.....	51
Pulse_low.....	51
Pulse_time.....	51
Vmeas.....	51
[Add Submodel].....	54

submodel_name	54
mode.....	54
[Submodel]	54
Submodel_type	54
[Submodel Spec]	54
V_trigger_r.....	54
V_trigger_f.....	54
Off_delay	54
[GND Pulse Table].....	59
[POWER Pulse Table]	59
[TTgnd]	59
[TTpower]	59
Table 6: V-T Behavioral Properties.....	63
[Ramp].....	63
dV/dt_r.....	63
dV/dt_f.....	63
R_load.....	63
Vmeas	63
Cref	63
Rref	63
Vref	63
[Rising Waveform] &.....	63
[Falling Waveform].....	63
R_fixture	63
C_fixture	63
L_fixture	63
V_fixture.....	63
V_fixture_min.....	63
V_fixture_max	63
R_dut.....	63
C_dut.....	63
L_dut.....	63
[Driver Schedule]	67
Rise_on_dly	67
Rise_off_dly.....	67
Fall_on_dly	67
Fall_off_dly.....	67
Table 7: Board Properties.....	69
[Begin Board Description]	69
[Manufacturer]	69
[Number of Pins].....	69
[Pin List].....	70
[Path Description]	70
Len	70
L, R, C.....	70
Fork.....	70

Endfork	70
Pin	70
Node.....	70
[Reference Designator Map]	75
[End Board Description]	75
[End].....	75
[END]	75

Acknowledgement:

The text of the IBIS specification, v3.2, was used verbatim extensively to create this document.

Purpose:

This document was created to separate out syntax rules, file formatting and examples and make those subjects more accessible to the user. This author has added not much commentary. But, the material of the IBIS spec has been reorganized and reformatted. The IBIS spec is organized around a set of [Keywords] and (in some cases) their subparameters.

I have reorganized those keywords into a set of 7 tables as follows:

- Table 1: General Rules - reserved words, ASCII characters, etc.
- Table 2: General Properties - "boilerplate."
- Table 3: Component Properties - supplier, voltage and temperature ranges.
- Table 4: Package and Pin Properties - connections and parasitics.
- Table 5: V-I Behavioral Properties - driver voltage-current capabilities, clamping, power bussing, model types, etc.
- Table 6: V-T Behavioral Properties - slew rates and switching speeds.
- Table 7: Electrical Board Description - abstracting a board as a component.

Most of the above tables are split apart into sections or subtables so as to bring technical notes and examples into close association with the listed keywords and examples.

An industry committee created the IBIS specification over a period of years. It is still a "work in progress" undergoing continuing modification. As this author sees it, the specification is in need of organization and a roadmap to its information since disparate elements are mixed together and separated into unrelated sections and specific information is not easily accessible.

This syntax guide is offered in the hope that it will aid the reader in understanding the IBIS specification. This guide is followed by an example of an IBIS model file used with the permission of TI semiconductor.

Table 1: General Rules

Keyword	Syntax	Rules	Notes
Format	ASCII, case sensitive except for reserved words and keywords. No special non-DOS characters allowed.	ASCII as defined in ANSI Standard X3.4-1986	
File Names	All lower case, ending in .ibs extension for model files, .pkg extension for separate package model files, and .ebd for electrical board description files. 8 characters max plus extension		
Reserved Words	POWER	Used with power supply pins	
	GND	Used with ground pins	
	NC	No-connect pins	
	NA	Used where data not available	
Line Length	80 characters max		
Comments	Default are lines that begin with “ ” (pipe)		
Keywords	Must be enclosed with square brackets [] and begin in column 1	Underscores and spaces are equivalent in keywords. Spaces not allowed in subparameter names.	
Allowed Scaling Factor Prefixes	T	Tera	Parser assumes volts, amperes, ohms, farads, henries & seconds if not specified
	G	Giga	
	M	Mega	
	k	Kilo	
	m	Milli	
	u	Micro	
	n	Nano	
	p	Pico	
	f	Femto	
	1.234e-12	scientific notation	
Tab characters	Allowed. But, to be avoided		
Temperature	Degrees Celsius		
Currents	Positive when their direction is into the component		

Table 2: General Properties

Keyword	Syntax	Rules	Notes
[IBIS Ver]	Informs parser of the IBIS template version	Must be first keyword. Can be preceded by comment lines	Example #1
[Comment Char]	The new character to be defined must be followed by the underscore character and the letters "char". Ex.: " _char" redundantly redefines the comment character to be the pipe character. The new comment character is in effect only following the [Comment Char] keyword.	Following characters <u>MAY NOT</u> be used: A B C D E F G H I J K L M N O P Q R S T U V W X Y Z a b c d e f g h i j k l m n o p q r s t u v w x y z 0 1 2 3 4 5 6 7 8 9 [] . _ / = + -	
[File Name]	All lower case, ending in .ibs extension for model files, .pkg extension for separate package model files, and .ebd for electrical board description files. 8 characters max plus extension	The file name must be the actual name of the file	Example #2
[File Rev]		Revision level is set at the discretion of the engineer defining the file. The following are recommended: 0.x silicon and file in development 1.x pre-silicon file data from silicon model only 2.x file correlated to silicon measurements 3.x mature product, no more changes likely	Example #3
[Date]	40 characters max	Latest file revision date	Example #4
[Source]	Originator of IBIS file	Optional	
[Notes]	Paragraph allowed		
[Copyright]			
[Disclaimer]			

#1 IBIS Ver

[IBIS Ver]	3.2	Used for template variations

#2 File Name

[File Name]	ver3_2.ibs

#3 File Rev

[File Rev]	1.0	Used for .ibs file variations
------------	-----	-------------------------------

#4 Date/Source/Notes/Disclaimer/Copyright

[Date]	January 15, 1999	The latest file revision date
[Source]	Put originator and the source of information here. For example: From silicon level SPICE model at Intel. From lab measurement at IEI. Compiled from manufacturer's data book at Quad Design, etc.	
[Notes]	Use this section for special notes related to the file.	
[Disclaimer]	This information is for modeling purposes only and is not guaranteed.	
	May vary by component	
[Copyright]	Copyright 1999, XYZ Corp., All Rights Reserved	

Table 3: Component Properties

Keyword	Syntax	Rules	Notes
[Component]	40 characters max. Blank characters allowed. NOTE: Blank characters not recommended due to usability issues.	In multiple device files each one must begin with its own Component keyword	Marks start of IBIS description. Example #5
	Si_location	Must be 'Pin' or 'Die'	Example #5
	Timing_location	Must be 'Pin' or 'Die'	Example #5
[Manufacturer]	40 characters max. Blank characters allowed		Example #6
[Voltage Range]	Note 1.	Provide actual voltages (not percentages) in the typ, min, max format. If the [Voltage Range] keyword is not present, then all four of these keywords described below must be present: [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], and [GND Clamp Reference]. If the [Voltage Range] is present, the other keywords are optional and may or may not be used as required. It is legal (although redundant) for an optional keyword to specify the same voltage as specified by the [Voltage Range] keyword.	Example #7
[Temperature Range]	Note 1.	List the actual die temperatures (not percentages) in the typ, min, max format. The [Temperature Range] keyword also describes the temperature range over which the various V/I curves and ramp rates were derived.	Example #8
[END]		Defines the end of the .ibs file.	

#5 Component

```
[Component]      7403398 MC452
|
Si_location      Pin      | Optional subparameters to give measurement
Timing_location  Die      | location positions
|
```

#6 Manufacturer

```
[Manufacturer]   Quality Semiconductors Ltd.
|
```

#7 Voltage Range

```
| variable          typ          min          max
[Voltage Range]    5.0V          4.5V          5.5V
|
```

#8 Temperature Range

```
| variable          typ          min          max
[Temperature Range] 27.0          -50          130.0
```

Table 4: Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Package]	R_pkg	Note 1.*	Example #9
	L_pkg		
	C_pkg		
[Pin]	5 characters max	1 st column	Note 2, Example #10
	signal_name	2 nd column, 20 characters max	
	model_name	3 rd column, 20 characters max: associates I/O [Model] keyword or GND, POWER, or NC below it.	
	R_pin	Note 1.	
	L_pin		
	C_pin		

(cont.)

Assumed: Consistent with IBIS syntax.

Note 1

Typical must be specified. If data for Min & Max columns is not available that must be noted with NA. Consists of 3 columns (typ-min-max) of 9 characters max each. On each line at least one space must separate each column entry from its neighbor.

#9 Package

[Package]			
variable	typ	min	max
R_pkg	250.0m	225.0m	275.0m
L_pkg	15.0nH	12.0nH	18.0nH
C_pkg	18.0pF	15.0pF	20.0pF

Note 2

Each line must have either 3 or 6 columns. If six are used they are used to override the default package parameters. If NA is used the default package parameters are still used. At least one space must separate each column.

#10 Pin

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
1	RAS0#	Buffer1		200.0m	5.0nH 2.0pF
2	RAS1#	Buffer2		209.0m	NA 2.5pF
3	EN1#	Input1		NA	6.3nH NA
4	A0	3-state			
5	D0	I/O1			
6	RD#	Input2		310.0m	3.0nH 2.0pF
7	WR#	Input2			
8	A1	I/O2			
9	D1	I/O2			
10	GND	GND		297.0m	6.7nH 3.4pF
11	RDY#	Input2			
12	GND	GND		270.0m	5.3nH 4.0pF
.					
.					
.					
18	Vcc3	POWER			
19	NC	NC			
20	Vcc5	POWER		226.0m	NA 1.0pF

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Package Model]	40 characters max. Blank characters allowed. Inserted as keyword within Component keyword. The [Package Model] keyword is optional. If more than the default RLC package model is desired, use the [Define Package Model] keyword.	The simulator will search for a matching package model name as an argument to a [Define Package Model] keyword in the current IBIS file first. If a match is not found, the simulator will look for a match in an external .pkg file. If the package model is in a separate .pkg file, it must be kept in the same directory as the .ibs file.	Note 10, Example #11
[Define Package Model]	40 characters max. Blank characters are allowed.	If the .pkg file has data for more than one package, each section must begin with a new [Define Package Model]. For every package model name defined under the [Package Model] keyword, there must be a matching [Define Package Model]	Example #12

(cont.)

Note 10

Use the [Package Model] keyword within a [Component] to indicate the package model for that part.

The specification permits .ibs files to contain the following additional list of package model keywords. Note that the actual package models can be in a separate <package_file_name>.pkg file or can exist in the IBIS files between the [Define Package Model]...[End Package Model] keywords for each package model that is defined. For reference, these keywords are listed below. Full descriptions follow:

[Define Package Model]	Required if the [Package Model] keyword is used
[Manufacturer]	(note a)
[OEM]	(note a)
[Description]	(note a)
[Number of Pins]	(note a)
[Pin Numbers]	(note a)
[Model Data]	(note a)
[Resistance Matrix]	Optional
[Inductance Matrix]	(note a)
[Capacitance Matrix]	(note a)
[Bandwidth]	Required (for Banded_matrix matrices only)
[Row]	(note a)
[End Model Data]	(note a)

[End Package Model] (note a)

(note a) Required when the [Define Package Model] keyword is used

When package model definitions occur within a .ibs file, their scope is "local" -- they are known only within that .ibs file and no other. In addition, within that .ibs file, they override any globally defined package models that have the same name.

USAGE RULES FOR THE .PKG FILE

Package models are stored in a file whose name looks like:
<filename>.pkg.

The <filename> provided must adhere to the General Syntax Rules. Use the ".pkg" extension to identify files containing package models. The .pkg file must contain all of the required elements of a normal .ibs file, including [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords.

All of the elements follow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .pkg file. The .pkg file is for package models only.

#11 Package Model

```
|                                     Package Model Example
|
| The following is an example of a package model file following the
| package modeling specifications. For the sake of brevity, an 8-pin
package
| has been described. For purposes of illustration, each of the
matrices is
| specified using a different format.
|
|=====
|
[IBIS Ver]      3.2
[File Name]     example.pkg
[File Rev]      0.1
[Date]          January 15, 1999
[Source]        Quality Semiconductors. Data derived from Helmholtz
                Inc.'s field solver using 3-D Autocad model from Acme
                Packaging.
[Notes]         Example of couplings in packaging
[Disclaimer]    The models given below may not represent any physically
                realizable 8-pin package. They are provided solely for
the
                purpose of illustrating the .pkg file format.
|
```



```

|=====
|
[Define Package Model]  QS-SMT-cer-8-pin-pkgs
[Manufacturer]          Quality Semiconductors Ltd.
[OEM]                  Acme Package Co.
[Description]          8-Pin ceramic SMT package
[Number Of Pins]       8
|
1
2
3
4
5
6
7
8
|
[Model Data]
|
| The resistance matrix for this package has no coupling
|
[Resistance Matrix]     Banded_matrix
[Bandwidth]            0
[Row] 1
10.0
[Row] 2
15.0
[Row] 3
15.0
[Row] 4
10.0
[Row] 5
10.0
[Row] 6
15.0
[Row] 7
15.0
[Row] 8
10.0
|
| The inductance matrix has loads of coupling
|
[Inductance Matrix]     Full_matrix
[Row] 1
3.04859e-07      4.73185e-08      1.3428e-08      6.12191e-09
1.74022e-07      7.35469e-08      2.73201e-08      1.33807e-08
[Row] 2
3.04859e-07      4.73185e-08      1.3428e-08      7.35469e-08
1.74022e-07      7.35469e-08      2.73201e-08
[Row] 3
3.04859e-07      4.73185e-08      2.73201e-08      7.35469e-08
1.74022e-07      7.35469e-08
[Row] 4
3.04859e-07      1.33807e-08      2.73201e-08      7.35469e-08
1.74022e-07
[Row] 5

```

```

4.70049e-07      1.43791e-07      5.75805e-08      2.95088e-08
[Row]    6
4.70049e-07      1.43791e-07      5.75805e-08
[Row]    7
4.70049e-07      1.43791e-07
[Row]    8
4.70049e-07
|
| The capacitance matrix has sparse coupling
|
[Capacitance Matrix]      Sparse_matrix
[Row]    1
1          2.48227e-10
2          -1.56651e-11
5          -9.54158e-11
6          -7.15684e-12
[Row]    2
2          2.51798e-10
3          -1.56552e-11
5          -6.85199e-12
6          -9.0486e-11
7          -6.82003e-12
[Row]    3
3          2.51798e-10
4          -1.56651e-11
6          -6.82003e-12
7          -9.0486e-11
8          -6.85199e-12
[Row]    4
4          2.48227e-10
7          -7.15684e-12
8          -9.54158e-11
[Row]    5
5          1.73542e-10
6          -3.38247e-11
[Row]    6
6          1.86833e-10
7          -3.27226e-11
[Row]    7
7          1.86833e-10
8          -3.38247e-11
[Row]    8
8          1.73542e-10
|
[End Model Data]
[End Package Model]
|
|=====

```

#12 Define Package Model

```

[Define Package Model]      QS-SMT-cer-8-pin-pkgs
|

```

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Manufacturer]	40 characters max. Blank characters are allowed.		Example #6
[OEM]	40 characters max. Blank characters are allowed.	This keyword is useful if the semiconductor vendor sells a single IC in packages from different manufacturers	Example #13
[Description]	The description must be less than 60 characters in length, must fit on a single line, and may contain spaces		Example #14
[Number of Pins]	The field must be a positive decimal integer		Example #15
[Pin Numbers]	5 characters max	Tells the parser the set of names that are used for the package pins, and to define an ordering of them. The first pin name given is the "lowest" pin, and the last pin given is the "highest."	Note 11. Example #16
	Len	*1 character max.	Note 11. Example #17
	L, R, C.	Note 1.	
	Fork		
	Endfork		

(cont.)

#13 OEM

[OEM] Acme Packaging Co.
|

#14 Description

[Description] 220-Pin Quad Ceramic Flat Pack
|

#15 Number Of Pins

[Number Of Pins] 128
|

Note 11

Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as there are pins (as given by the preceding [Number of Pins].) All the subparameter listed under [Pin Numbers] actually describe a Section as in [Number of Sections].

Specifying a Len or L/R/C value of zero is allowed. If Len = 0 is specified, then the L/R/C values are the total for that section. If a non-zero length is specified, then the total L/R/C for a section is calculated by multiplying the value of the Len subparameter by the value of the L, R, or C subparameter. However, if a non-zero length section is specified, the L and C for that section should be treated as distributed elements.

Using The Subparameters to Describe Package Stub Sections:

A section description begins with the Len subparameter and ends with the slash (/) character. The value of the Len, L, R, and C subparameters and the subparameter itself are separated by an equals sign (=); whitespace around the equals sign is optional. The Fork and Endfork subparameters are placed between section descriptions (i.e. between the concluding slash of one section and the 'Len' parameter that starts another). A particular section description can contain no data (i.e. the description is given as 'Len = 0 /').

Legal Subparameter Combinations for Section Descriptions:

A) A single Len = 0 subparameter, followed by a slash. This is used to describe a section with no data.

B) Len, and one or more of the L, R and C subparameters. If the Len subparameter is given as zero, then the L/R/C subparameters represent lumped elements. If the Len subparameter is non-zero, then the L/R/C subparameters represent distributed elements.

C) Single Fork or Endfork subparameter. Normally, a package stub is described as several sections, with the Fork and Endfork subparameters surrounding a group of sections in the middle of the complete package stub description. However, it is legal for the Fork/Endfork subparameters to appear at the end of a section description. The package pin is connected to the last section of a package stub description not surrounded by a Fork/Endfork statements.

Package Stub Boundaries:

A package stub description starts at the connection to the die and ends at the point at which the package pin interfaces with the board or substrate the IC package is mounted on. Note that in the case of a component with thru-hole pins, the package stub description should include only the portion of the pin not physically inserted into the board or socket. However, it is legal for a package stub description to include both the component and socket together if this is how the component is intended to be used.

#16 Pin Numbers

```
|
| A three-section package stub description that includes a bond wire
| (lumped inductance), a trace (treated as a transmission line with DC
| resistance), and a pin modeled as a lumped L/C element.
|
[Pin Numbers]
A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
|
| Pin A2 below has a section with no data
|
A2 Len=0 L=1.2n/ Len=0/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n
C=1.0p/
|
| A section description using the Fork and Endfork subparameters. Note
| that the indentation of the Fork and Endfork subparameters are for
| readability are not required.
|
A1 Len=0 L=2.3n /          | bondwire
Len=1.2 L=1.0n C=2.5p /    | first section
  Fork                    | indicates the starting of a branch
  Len=1.0 L=2.0n C=1.5p /  | section
  Endfork                  | ending of the branch
Len=0.5 L=1.0 C=2.5p/      | second section
Len=0.0 L=1.5n /           | pin
|
| Here is an example where the Fork/Endfork subparameters are at the
| end of a package stub description
|
B13 Len=0 L=2.3n /          | bondwire
Len=1.2 L=1.0n C=2.5p /    | first section
Len=0.5 L=1.0 C=2.5/       | second section, pin connects here
Fork                        | indicates the starting of a branch
Len=1.0 L=2.0n C=1.5p /    | section
Endfork                     | ending of the branch
|
```

#17 Number of Sections

```
[Number Of Sections]    3
|
```

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Number Of Sections]	The argument is a + integer >0. *1 character max. If used, this keyword must appear before [Pin Numbers]	A section description begins with Len and ends with a slash (/) character.	Example #17
[Model Data]		Indicates the beginning of the formatted package model data, which can include the [Resistance Matrix], [Inductance Matrix], [Capacitance Matrix], [Bandwidth], and [Row] keywords	Note 12, Example #18

(cont.)

Note 12

The data is a set of 3 matrices: the resistance (R), inductance (L), and capacitance (C) matrices. Each matrix can be formatted differently (see below). Use one of the matrix keywords below to mark the beginning of each new matrix.

[Resistance Matrix] is optional. If it is not present, its entries are assumed to be zero. [Inductance Matrix] and [Capacitance Matrix] are required.

For each [Resistance Matrix], [Inductance Matrix], or [Capacitance Matrix] a different format can be used for the data. The choice of formats is provided to satisfy different simulation accuracy and speed requirements. Also, there are many packages in which the resistance matrix can have no coupling terms at all. In this case, the most concise format (Banded_matrix) can be used.

One common aspect of all the different formats is that they exploit the symmetry of the matrices they describe. This means that the entries below the main diagonal of the matrix are identical to the corresponding entries above the main diagonal. Therefore, only roughly one-half of the matrix needs to be described. By convention, the main diagonal and the UPPER half of the matrix are provided.

In the following text, we use the notation [I, J] to refer to the entry in row I and column J of the matrix. Note that I and J are allowed to be alphanumeric strings as well as integers. An ordering of these strings is defined in the [Pin Numbers] section. In the following text, "Row 1", means the row corresponding to the first pin.

Also note that the numeric entries of the RLC matrices are standard IBIS floating point numbers. As such, it is permissible to use metric

"suffix" notation. Thus, an entry of the C matrix could be given as 1.23e-12 or as 1.23p or 1.23pF.

#18 Model Data/End Model Data

```
[Model Data]
|
[End Model Data]
|
```

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Resistance Matrix]	See [Inductance Matrix].	Optional, if not present its entries are assumed to be 0	Example #19
[Inductance Matrix]	The subparameters below mark the beginning of a matrix and specify how the matrix data is to be formatted.	For each matrix keyword, use only one of the subparameters. After each of these subparameters, insert the matrix data in the appropriate format	Example #19
	Banded_matrix	Indicates the bandwidth of the matrix. The bandwidth field must be a nonnegative integer. This keyword must occur after the [Resistance Matrix], etc. keywords, and before the matrix data is given.	Note 14. Example #19
	Sparse_matrix	A Sparse_matrix is expected to consist mostly of zero-valued entries, except for a few non-zeros.	Note 15. Example #19
	Full_matrix	When the Full_matrix format is used, the couplings between every pair of elements is specified explicitly.	Note 13. Example #19

(cont.)

Note 13. Full_matrix

When the Full_matrix format is used, the couplings between every pair of elements is specified explicitly. Assume that the matrix has N rows and N columns. The Full_matrix is specified one row at a time, starting with Row 1 and continuing down to Row N.

Each new row is identified with the Row keyword.

Following a [Row] keyword is a block of numbers that represent the entries for that row. Suppose that the current row is number M. Then the first number listed is the diagonal entry, [M,M]. Following this number are the entries of the upper half of the matrix that belong to row M:

[M, M+1], [M, M+2], ... up to [M,N]

For even a modest-sized package, this data will not all fit on one line. You can break the data up with new-line characters so that this limit is observed.

An example:

Suppose the package has 40 pins and that we are currently working on Row 19. There is 1 diagonal entry, plus $40 - 19 = 21$ entries in the upper half of the matrix to be specified, for 22 entries total. The data might be formatted as follows:

```
[Row]    19
5.67e-9  1.1e-9  0.8e-9  0.6e-9  0.4e-9  0.2e-9  0.1e-9  0.09e-9
8e-10    7e-10  6e-10  5e-10  4e-10  3e-10  2e-10  1e-10
9e-11    8e-11  7e-11  6e-11  5e-11  4e-11
```

In the above example, the entry 5.67e-9 is on the diagonal of row 19.

Observe that Row 1 always has the most entries, and that each successive row has one fewer entry than the last; the last row always has just a single entry.

Note 14. Banded_matrix

A Banded_matrix is one whose entries are guaranteed to be zero if they are farther away from the main diagonal than a certain distance, known as the "bandwidth." Let the matrix size be N x M, and let the bandwidth be B. An entry [I,J] of the matrix is zero if:

$$| I - J | > B$$

where |.| denotes the absolute value.

The Banded_matrix is used to specify the coupling effects up to B pins on either side. Two variations are supported. One allows for the coupling to circle back on itself. This is technically a simple form of a bordered block diagonal matrix. However, its data can be

completely specified in terms of a Banded_matrix for an $N \times M$ matrix consisting of N rows and $M = N + B$ columns. The second variation is just in terms of an $N \times N$ matrix where no circle back coupling needs to be specified.

The bandwidth for a Banded_matrix must be specified using the [Bandwidth] keyword.

Specify the banded matrix one row at a time, starting with row 1 and working up to higher rows. Mark each row with the [Row] keyword, as above. As before, symmetry is exploited: do not provide entries below the main diagonal.

For case where coupling can circle back on itself, consider a matrix of N pins organized into N rows 1 ... N and M columns 1 ... N , 1 ... B . The first row only needs to specify the entries [1,1] through [1,1+B] since all other entries are guaranteed to be zero. The second row will need to specify the entries [2,2] through [2,2+B], and so on. For row K the entries [K,K] through [K,K+B] are given when $K + B$ is less than or equal to the size of the matrix N . When $K + B$ exceeds N , the entries in the last columns 1 ... B specify the coupling to the first rows. For row K , the entries [K,K] ... [K,N] [K,1] ... [K,R] are given where $R = \text{mod}(K + B - 1, N) + 1$. All rows will contain $B + 1$ entries.

To avoid redundant entries, the bandwidth is limited to $B \leq \text{int}((N - 1) / 2)$.

For the case where coupling does not circle back on itself, the process is modified. Only N columns need to be considered. When $K + B$ finally exceeds the size of the matrix N , the number of entries in each row starts to decrease; the last row (row N) has only 1 entry. This construction constrains the bandwidth to $B < N$.

As in the Full_matrix, if all the entries for a particular row do not fit into a single 80-character line, the entries can be broken across several lines.

It is possible to use a bandwidth of 0 to specify a diagonal matrix (a matrix with no coupling terms.) This is sometimes useful for resistance matrices.

Note 15. Sparse_matrix

A Sparse_matrix is expected to consist mostly of zero-valued entries, except for a few nonzeros. Unlike the Banded_matrix, there is no restriction on where the nonzero entries can occur. This feature is useful in certain situations, such as for Pin Grid Arrays (PGAs).

As usual, symmetry can be exploited to reduce the amount of data by eliminating from the matrix any entries below the main diagonal.

An $N \times N$ Sparse_matrix is specified one row at a time, starting with row 1 and continuing down to row N . Each new row is marked with [Row] keyword, as in the other matrix formats.

Data for the entries of a row is given in a slightly different format, however. For the entry [I, J] of a row, it is necessary to explicitly list the name of pin J before the value of the entry is given. This specification serves to indicate to the parser where the entry is put into the matrix.

The proper location is not otherwise obvious because of the lack of restrictions on where nonzeros can occur. Each (Index, Value) pair is listed upon a separate line. An example follows:

Suppose that row 10 has nonzero entries [10,10], [10,11], [10,15], and [10,25]. The following row data would be provided:

```
[Row]    10
| Index      Value
10         5.7e-9
11         1.1e-9
15         1.1e-9
25         1.1e-9
```

Note that each of the column indices listed for any row must be greater than or equal to the row index, because they always come from the upper half of the matrix. When alphanumeric pin names are used, special care must be taken to ensure that the ordering defined in the [Pin Numbers] section is observed.

With this convention, please note that the nth row of an N x N matrix has just a single entry (the diagonal entry).

#19 Resistance/Inductance/Capacitance Matrix

```
[Resistance Matrix]    Banded_matrix
[Inductance Matrix]    Sparse_matrix
[Capacitance Matrix]   Full_matrix
|
```

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Capacitance Matrix]	See [Inductance Matrix]		Example #19
[Row]	5 Characters max	Indicates the beginning of a new row (line) of the matrix. The argument must be one of the pin numbers listed under the [Pin Numbers] keyword. A row/line in a matrix may need to be longer than 80 characters. If so, use ASCII line continuation characters.	Example #20
[Bandwidth]	Given an entry with index [I,J] of the matrix: Bandwidth = I - J where . denotes the absolute value	A banded matrix is one whose entries are guaranteed to be zero if they are further away from the main diagonal than a certain distance known as the “bandwidth”	Example #21
[End Model Data]		Marks the end of the [Model Data]	Example #18

(cont.)

#20 Row

```
[Row]      19
5.67e-9    1.1e-9    0.8e-9    0.6e-9    0.4e-9    0.2e-9    0.1e-9    0.09e-9
8e-10      7e-10     6e-10     5e-10     4e-10     3e-10     2e-10     1e-10
9e-11      8e-11     7e-11     6e-11     5e-11     4e-11
|
```

#21 Bandwidth

```
[Bandwidth]      10
|
```

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Pin Mapping]	5 characters max	Rules are complex – see note 3. If [Pin Mapping] is present, then the bus connections for EVERY pin listed in the [Pin] section must be given.	Note 3, Example #22
	pulldown_ref: 15 characters max		
	pullup_ref: 15 characters max		
	gnd_clamp_ref: 15 characters max		
	power_clamp_ref: 15 characters max		

(cont.)

Note 3.

Each power and ground bus is given a unique name. The first column contains a pin number. Each pin number must match one of the pin numbers declared previously in the [Pin] section of the IBIS file. The second column, pulldown_ref, designates the ground bus connections for that pin. Here the term ground bus can also mean another power bus. The third column pullup_ref designates the power bus connection. The fourth and fifth columns gnd_clamp_ref and power_clamp_ref contain entries, if needed; to specify different ground bus and power bus connections than those previously specified.

If the [Pin Mapping] keyword is present, then the bus connections for EVERY pin listed in the [Pin] section must be given.

Each line must contain either three or five columns. Use the NC reserved word for entries that are not needed or that follow the conditions below:

All entries with identical labels are assumed to be connected. Each unique entry label must connect to at least one pin whose model_name is POWER or GND.

If a pin has no connection, then both the pulldown_ref and pullup_ref subparameters for it will be NC.

GND and POWER pin entries and buses are designated by entries in either the pulldown_ref or pullup_ref columns.

There is no implied association to any column other than through explicit designations in other pins.

For any other type of pin, the pulldown_ref column contains the power connection for the [Pulldown] table for non-ECL type [Models]. This is also the power connection for the

[GND Clamp] table and the [Rgnd] model unless overridden by a specification in the gnd_clamp_ref column.

Also, the pullup_ref column contains the power connection for the [Pullup] table and, for ECL type models, the [Pulldown] table. This is also the power connection for the [POWER Clamp] table and the [Rpower] model unless overridden by a specification in the power_clamp_ref column.

When 5 columns are specified, the headings gnd_clamp_ref and power_clamp_ref must be used. Otherwise, these headings can be omitted.

#22 Pin Mapping

[Pin Mapping]	pulldown_ref	pullup_ref	gnd_clamp_ref	power_clamp_ref
1	GNDBUS1	PWRBUS1	Signal pins & their assoc. ground and power connections GNDCLMP PWRCLAMP GNDCLMP PWRCLAMP NC PWRCLAMP GNDCLMP NC Some possible clamp connect. are shown above for illus. purposes	
2	GNDBUS2	PWRBUS2		
3	GNDBUS1	PWRBUS1		
4	GNDBUS2	PWRBUS2		
5	GNDBUS2	PWRBUS2		
6	GNDBUS2	PWRBUS2		
.				
.				
.				
11	GNDBUS1	NC	One set of ground connect.	
12	GNDBUS1	NC	NC indicates no connect to	
13	GNDBUS1	NC	power bus.	
.				
21	GNDBUS2	NC	Second set of gnd connect.	
22	GNDBUS2	NC		
23	GNDBUS2	NC		
.				
31	NC	PWRBUS1	One set of power connect.	
32	NC	PWRBUS1	NC indicates no connect to	
33	NC	PWRBUS1	ground bus.	
.				
41	NC	PWRBUS2	Second set of power connect.	
42	NC	PWRBUS2		
43	NC	PWRBUS2		
.				
51	GNDCLMP	NC	Additional power connections	
52	NC	PWRCLMP	for clamps	

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Rac]	Note 1*	The R and C of an AC terminator if present	Note 4, Example #23
[Cac]			
[Rgnd]			
[Rpower]			
[Diff Pin]	5 characters max	Complex, see note 7, Example #24	Note 7, Example #24
inv_pin:			
inverse pin. 5 characters max			
vdiff:			
differential offset volt. Note 1.			
tdelay_typ:			
differential offset time delay. Note 1.			
tdelay_min:			
ibid - min. Note 1.			
Tdelay_max:			
ibid - min. Note 1.			

(cont.)

* Assumed: Consistent with IBIS syntax.

Note 4

For each keyword, the three columns hold the typical, minimum, and maximum values. The three entries for R(typ), R(min), and R(max), or the three entries for C(typ), C(min), and C(max) must be placed on a single line and must be separated by at least one white space or tab character. All three columns are required under these keywords. However, data is only required in the typical column. If minimum and/or maximum values are not available, the reserved word "NA" must be used indicating the R(typ) or C(typ) value by default.

It should be noted that [Rpower] is connected to 'Vcc' and [Rgnd] is connected to 'GND'. However, [GND Clamp Reference] voltages, if defined, apply to [Rgnd]. [POWER Clamp Reference] voltages, if defined, apply to [Rpower]. Either or both [Rgnd] and [Rpower] may be defined and may coexist with [GND Clamp] and [POWER Clamp] tables. If the terminator consists of a series R and C (often referred to as either an AC or RC terminator), then both [Rac] and [Cac] are required. When [Rgnd], [Rpower], or [Rac] and [Cac] are specified, the Model_type must be Terminator.

[illegible]

#23 Rgnd/Rpower/Rac/Cac

variable	R(typ)	R(min)	R(max)
[Rgnd]	330ohm	300ohm	360ohm
Parallel Terminator			
[Rpower]	220ohm	200ohm	NA
[Rac]	30ohm	NA	NA
variable	C(typ)	C(min)	C(max)
AC terminator			
[Cac]	50pF	NA	NA

Note 7.

Enter only differential pin pairs. The first column, [Diff Pin], contains a non-inverting pin number. The second column, inv_pin, contains the corresponding inverting pin number for I/O output. Each pin number must match the pin numbers declared previously in the [Pin] section of the IBIS file. The third column, vdiff, contains the specified output and differential threshold voltage between pins if the pins are Input or I/O model types. For output only differential pins, the vdiff entry is 0 V. The fourth, fifth, and sixth columns, tdelay_typ, tdelay_min, and tdelay_max, contain launch delays of the non-inverting pins relative to the inverting pins. The values can be of either polarity.

If a pin is a differential input pin, the differential input threshold (vdiff) overrides and supersedes the need for Vinh and Vinl. If vdiff is not defined for a pin that is defined as requiring a Vinh by its [Model] type, vdiff is set to the default value of 200 mV.

The output pin polarity specification in the table overrides the [Model] Polarity specification such that the pin in the [Diff Pin] column is Non-Inverting and the pin in the inv_pin column is Inverting. This convention enables one [Model] to be used for both pins.

Each line must contain either four or six columns. If "NA" is entered in the vdiff, tdelay_typ, or tdelay_min columns, its entry is interpreted as 0 V or 0 ns. If "NA" appears in the tdelay_max column, its value is interpreted as the tdelay_typ value. When using six columns, the headers tdelay_min and tdelay_max must be listed. Entries for the tdelay_min column are based on minimum magnitudes; and tdelay_max column, maximum magnitudes. One entry of vdiff, regardless of its polarity, is used for difference magnitudes.

#24 Differential Pins

[Diff Pin]	inv_pin	vdiff	tdelay_typ	tdelay_min	tdelay_max
3	4	150mV	-1ns	0ns	-2ns
Input or I/O pair					
7	8	0V	1ns	NA	NA
Output* pin pair					
9	10	NA	NA	NA	NA
Output* pin pair					
16	15	200mV	1ns	Input or I/O pin pair	
20	19	0V	NA	Output* pin pair, tdelay = 0	
22	21	NA	NA	Output*, tdelay = 0	
				* Could be Input or I/O with	
				vdiff = 0	

Table 4 (cont.): Package and Pin Properties

Keyword	Syntax	Rules	Notes
[Series Pin Mapping]	5 characters max	Associates 2 pins joined by a series model	Note 16. Example #25
	pin_2: 5 characters max		
	model_name: 20 characters max		
	function_table_group: 20 characters max		
[Series Switch Groups]	On, Off	Defines allowable switching combinations (states) of the groups in function_table_group	Note 17. Example #26
[End Package Model]		Indicates the end of the formatted model data	Example #27

Note 16

Enter only series pin pairs. The first column, [Series Pin Mapping], contains the series pin for which input impedances are measured. The second column, pin_2, contains the other connection of the series model. Each pin must match the pin names declared previously in the [Pin] section of the IBIS file. The third column, model_name, associates the Series or Series_switch model for the pair of pins in the first two columns. The fourth column, function_table_group, contains an alphanumeric designator string to associate those sets of Series_switch pins that are switched together.

Each line must contain either three or four columns. When using four columns, the header function_table_group must be listed.

One possible application is to model crossbar switches where the straight through On paths are indicated by one designator and the cross over On paths are indicated by another designator. If the model referenced is a Series model, then the function_table_group entry is omitted.

If the model_name is for a non-symmetrical series model, then the order of the pins is important. The [Series Pin Mapping] and pin_2 entries must be in the columns that correspond with Pin 1 and Pin 2 of the referenced model.

This mapping covers only the series paths between pins. The package parasitics and any other elements such as additional capacitance or clamping circuitry are defined by the model_name that is referenced in the [Pin] keyword. The model_names under the [Pin] keyword that are also referenced by the [Series Pin Mapping] keyword may include any legal model or reserved model except for Series and Series_switch models. Normally the pins will reference a [Model] whose Model_type is 'Terminator'. For example, a Series_switch model may contain

Terminator models on EACH of the pins to describe both the capacitance on each pin and some clamping circuitry that may exist on each pin. In a similar manner, Input, I/O or Output models may exist on each pin of a Series model that is serving as a differential termination.

#25 Series Pin Mapping

[Series Pin Mapping]	pin_2	model_name	function_table_group
2	3	CBTSeries	1 4 independent groups
5	6	CBTSeries	2
9	8	CBTSeries	3
12	11	CBTSeries	4
22	23	CBTSeries	5 Straight thru path
25	26	CBTSeries	5
22	26	CBTSeries	6 Cross over path
25	23	CBTSeries	6
32	33	Fixed_series	No group needed

Note 17

Each state line contains an allowable configuration. A typical state line will start with 'On' followed by all of the on-state group names or an 'Off' followed by all of the off-state group names. Only one of 'On' or 'Off' is required since the undefined states are presumed to be opposite of the explicitly defined states. The state line is terminated with the slash '/', even if it extends over several lines to fit within the 80 character column width restriction.

The group names in the function_table_group are used to associate switches whose switching action is synchronized by a common control function. The first line defines the assumed (default) state of the set of series switches. Other sets of states are listed and can be selected through a user interface or through automatic control.

#26 Series Switch Groups

```
[Series Switch Groups]
| Function Group States
On 1 2 3 4 /           | Default setting is all switched On.
|
Off 1 2 3 4 /          | All Off setting.
On 1 /                 | Other possible combinations below.
On 2 /
On 3 /
On 4 /
On 1 2 /
On 1 3 /
On 1 4 /
```

On 2 3 /	
On 2 4 /	
On 3 4 /	
On 1 2 3 /	
On 1 2 4 /	
On 1 3 4 /	
On 2 3 4 /	
Off 4 /	The last four lines above could have been replaced
Off 3 /	with these four lines with the same meaning.
Off 2 /	
Off 1 /	
On 5 /	Crossbar switch straight through connection
On 6 /	Crossbar cross over connection
Off 5 6 /	Crossbar open switches

#27 End Package Model

```
[End Package Model]
|
```

Table 5: V-I Behavioral Properties

Keyword	Syntax	Rules	Notes
[Model]	20 characters max	Each model type must begin with the keyword [Model]. The model name must match the one that is listed under the [Pin] keyword. A .ibs file must contain enough [Model] keywords to cover all of the model names specified under the [Pin] keyword, except for those model names that use reserved words (POWER, GND and NC). Model names with reserved words are an exception and they do not have to have a corresponding [Model] keyword.	Note 1 & Note 5. Example #28
	Model_type	Model_type must be one of the following: Input, Output, I/O, 3-state, Open_drain, I/O_open_drain, Open_sink, I/O_open_sink, Open_source, I/O_open_source, Input_ECL, Output_ECL, I/O_ECL, Terminator, Series or Series_switch.	
	C_comp : Note 1*.	C_comp defines the silicon die capacitance. This value should not include the capacitance of the package. C_comp is allowed to use "NA" for the min and max values only.	
	Polarity	Non-Inverting or Inverting	
	Enable	Active-High or Active-Low.	
	Vinl Note 1*.	Input Vt low if present.	
	Vinh Note 1*.	Input Vt high if present	

(cont.)

* Assumed: Consistent with IBIS spec.

Note 5

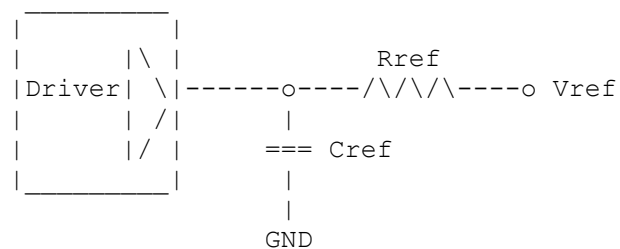
Special usage rules apply to the following. Some definitions are included for clarification:

Input I/O I/O_open_drain I/O_open_sink I/O_open_source	These model types must have Vinl and Vinh defined. If they are not defined, the parser issues a warning and the default values of Vinl = 0.8 V and Vinh = 2.0 V are assumed.
Input_ECL I/O_ECL	These model types must have Vinl and Vinh defined. If they are not defined, the parser issues a warning and the default values of Vinl = -1.475 V and Vinh = -1.165 V are assumed.
Terminator	This model type is an input-only device that can have analog loading effects on the circuit being simulated but has no digital logic thresholds. Examples of Terminators are: capacitors, termination diodes, and pull-up resistors.
Output	This model type indicates that an output always sources and/or sinks current and cannot be disabled.
3-state	This model type indicates that an output can be disabled, i.e. put into a high impedance state.
Open_sink Open_drain	These model types indicate that the output has an OPEN side (do not use the [Pullup] keyword, or if it must be used, set I = 0 mA for all voltages specified) and the output SINKS current. Open_drain model type is retained for backward compatibility.
Open_source	This model type indicates that the output has an OPEN side (do not use the [Pulldown] keyword, or if it must be used, set I = 0 mA for all voltages specified) and the output SOURCES current.
Input_ECL Output_ECL I/O_ECL	These model types specify that the model represents an ECL type logic that follows different conventions for the [Pulldown] keyword.
Series	This model type is for series models that can be described by [R Series], [L Series], [Rl Series], [C Series], [Lc Series], [Rc Series], [Series Current] and [Series MOSFET] keywords
Series_switch	This model type is for series switch models that can be described by [On], [Off], [R Series], [L Series], [Rl Series], [C Series], [Lc Series], [Rc Series], [Series Current] and [Series MOSFET] keywords

The Model_type and C_comp subparameters are required. The

Polarity, Enable, Vinl, Vinh, Vmeas, Cref, Rref, and Vref subparameters are optional. C_comp defines the silicon die capacitance. This value should not include the capacitance of the package. C_comp is allowed to use "NA" for the min and max values only. The Polarity subparameter can be defined as either Non-Inverting or Inverting, and the Enable subparameter can be defined as either Active-High or Active-Low.

The Cref and Rref subparameters correspond to the test load that the semiconductor vendor uses when specifying the propagation delay and/or output switching time of the model. The Vmeas subparameter is the reference voltage level that the semiconductor vendor uses for the model. Include Cref, Rref, Vref, and Vmeas information to facilitate board-level timing simulation. The assumed connections for Cref, Rref, and Vref are shown in the following diagram:



A complete [Model] description normally contains the following keywords: [Voltage Range], [Pullup], [Pulldown], [GND Clamp], [POWER Clamp], and [Ramp]. A Terminator model uses one or more of the [Rgnd], [Rpower], [Rac], and [Cac]. However, some models may have only a subset of these keywords. For example, an input structure normally only needs the [Voltage Range], [GND Clamp], and possibly the [POWER Clamp] keywords. If one or more of [Rgnd], [Rpower], [Rac], and [Cac] keywords are used, then the Model_type must be Terminator.

#28 Model

Signals	CLK1, CLK2,...	Optional signal list, if desired
[Model]	Clockbuffer	
Model_type	I/O	
Polarity	Non-Inverting	
Enable	Active-High	
Vinl = 0.8V		input logic "low" DC voltage, if any
Vinh = 2.0V		input logic "high" DC voltage, if any
Vmeas = 1.5V		Reference voltage for timing measurements
Cref = 50pF		Timing specification test load capacitance value
Rref = 500		Timing specification test load resistance value
Vref = 0		Timing specification test load voltage
variable	typ	min
C_comp	12.0pF	10.0pF
		max
		15.0pF

Table 5 (cont.): V-I Properties

Keyword	Syntax	Rules	Notes
[On]	On-state electrical models are positioned under [On]	Note 23	Example #29
[Off]	Off-state electrical models are positioned under [Off]		
[R Series]	Note 1.*	The data for these keywords allow the definition of Series or Series_switch R, L, or C paths. Note 24	Example #30
[L Series]			
[C Series]			
[Rl Series]			
[Rc Series]			
[Lc Series]			
[Series Current]	Pins 1 and 2 are listed under the [Series Pin Mapping] keyword under columns [Series Pin Mapping] and pin_2 respectively.	The data point under this keyword define the V-I tables for voltages measured at pin1 w.r.t. pin2. Currents are + if they flow into pin1.	Note 25. Example #31
[Series MOSFET]	Pins 1 and 2 are listed under the [Series Pin Mapping] keyword under columns [Series Pin Mapping] and pin_2 respectively.	The data point under this keyword define the V-I tables for voltages measured at pin2 for a given Vds setting. Currents are + if they flow into pin1.	Note 26. Example #32
	Vds Note 1*.		

(cont.)

* Assumed: Consistent with IBIS syntax

Note 23

These keywords are only valid for Series_switch Model_types. Only keywords associated with Series_switch electrical models are permitted under [On] or [Off]. The Series electrical models describe the path for one state only and do not use the [On] and [Off] keywords.

In Series_switch models, [On] or [Off] must be positioned before any of the [R Series], [L Series], Rl Series], [C Series], [Lc Series], [Rc Series], [Series Current], and [Series MOSFET] keywords. There is no provision for any of these keywords to be defined once, but to apply to both states.

#29 On/Off

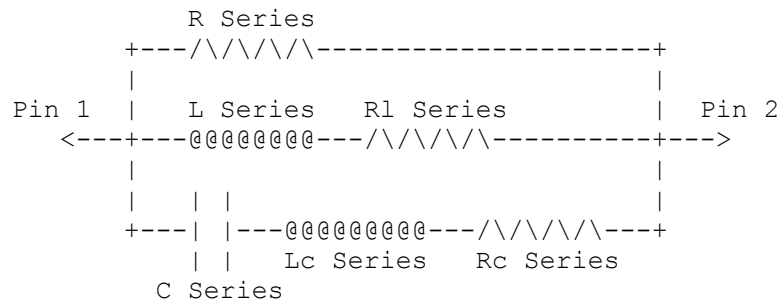
```
[On]
| ... On state keywords such as [R Series], [Series Current], [Series
|     MOSFET]
[Off]
| ... Off state keywords such as [R Series], [Series Current]
|
```

Note 24

This series RLC model is defined to allow IBIS to model simple passive models and/or parasitics.

These keywords are valid only for Series or Series_switch Model_types.

The model is:



[Rl Series] shall be defined only if [L Series] exists. [Rl Series] is 0 ohms if it is not defined in the path. [Rc Series] and [Lc Series] shall be defined only if [C Series] exists. [Rc Series] is 0 ohms if it is not defined in the path. [Lc Series] is 0 henries if it is not defined in the path. C_comp values are ignored for these keywords.

#30 R/L/Rl/C/Rc/Lc Series

variable	R(typ)	R(min)	R(max)	
[R Series]	8ohm	6ohm	12ohm	
variable	L(typ)	L(min)	L(max)	
[L Series]	5nH	NA	NA	
variable	R(typ)	R(min)	R(max)	
[Rl Series]	4ohm	NA	NA	
variable	C(typ)	C(min)	C(max)	Other elements
[C Series]	50pF	NA	NA	are 0 impeded.

Note 25

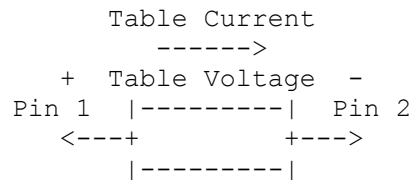
The first column contains the voltage value, and the remaining columns hold the typical, minimum, and maximum current values. The four entries, Voltage, I(typ), I(min), and I(max) must be placed on a single line and must be separated by at least one white space or tab character.

All four columns are required under these keywords. However, data is only required in the typical column. If minimum and/or maximum current values are not available, the reserved word "NA" must be used. "NA" can be used for currents in the typical column, but numeric values MUST be specified for the first and last voltage points on any V/I table. Each V/I table must have at least 2, but not more than 100, voltage points.

There is no monotonicity requirement. However the model supplier should realize that it may not be possible to derive a behavioral model from non-monotonic data. These keywords are valid only for Series or Series_switch. C_comp values are ignored for [Series Current] models.

Model_types.

The model is:



#31 Series Current

[Series Current]				
Voltage	I(typ)	I(min)	I(max)	
-5.0V	-3900.0m	-3800.0m	-4000.0m	
-0.7V	-80.0m	-75.0m	-85.0m	
-0.6V	-22.0m	-20.0m	-25.0m	
-0.5V	-2.4m	-2.0m	-2.9m	
-0.4V	0.0m	0.0m	0.0m	
5.0V	0.0m	0.0m	0.0m	

|

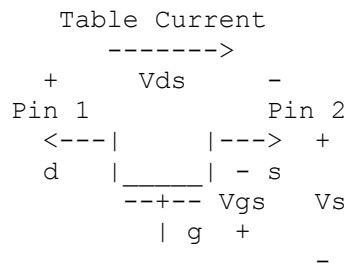
Note 26

The first column contains the voltage value, and the three remaining columns hold the typical, minimum, and maximum current values. The four entries, Voltage, I(typ), I(min), and I(max) must be placed on a single line and must be separated by at least one white space or tab character.

All four columns are required under these keywords. However, data is only required in the typical column. If minimum and/or maximum current values are not available, the reserved word "NA" must be used. "NA" can be used for currents in the typical column, but numeric values MUST be specified for the first and last voltage points on any V/I table. Each V/I table must have at least 2, but not more than 100, voltage points.

There is no monotonicity requirement. However the model supplier should realize that it may not be possible to derive a behavioral model from non-monotonic data.

The model is:



Vg = [Voltage Range] = Vcc
Vgs = Table Voltage = Vtable = Vcc - Vs
Ids = Table Current for a given Vcc and Vds

Internal logic that is generally referenced to the power rail is used to set the MOSFET switch to its 'On' state. Thus the [Voltage Range] settings provide the assumed gate voltages. If the [POWER Clamp reference] exists, it overrides the [Voltage Range] value. The table entries are actually the Vgs values referenced to the power rail. The polarity conventions are identical with those used for other tables that are referenced to power rails. Thus the voltage column can be viewed as a table defining the source voltages Vs according to the convention: Vtable = Vcc - Vs.

If the switch is used in an application such as interfacing between 3.3 V and 5.0 V logic, the Vcc may be biased at a voltage (such as 4.3 V) that is different from a power rail voltage (such as 5.0 V) used to create the model. Just readjust the [Voltage Range] entries (or [POWER Clamp Reference] entries).

One fundamental assumption in the MOSFET switch model is that it operates in a symmetrical manner. The tables and expressions are given assuming that Vd >= Vs. If Vd < Vs, then apply the same relationships under the assumption that the source and drain nodes are interchanged.

A consequence of this assumption is that the Vds subparameter is constrained to values $V_{ds} > 0$. It is assumed that with $V_{ds} = 0$ the currents will be 0 mA. A further consequence of this assumption that would be embedded in the analysis process is that the voltage table is based on the side of the model with the lowest voltage (and that side is defined as the source). Thus the analysis must allow current to flow in both directions, as would occur due to reflections when the switch is connected in series with an unterminated transmission line.

The model data is used to create an On state relationship between the actual drain to source current, i_{ds} , and the actual drain to source voltage, v_{ds} :

$i_{ds} = f(v_{ds})$.

This functional relationship depends on the actual source voltage V_s and can be expressed in terms of the corresponding table currents associated with V_s (and expressed as a function of V_{gs}).

If only one [Series MOSFET] table is supplied (as a first order approximation), the functional relationship is assumed to be linearly related to the table drain to source current, I_{ds} , for the given V_{ds} subparameter value and located at the existing gate to source voltage value V_{gs} . This table current is denoted as $I_{ds}(V_{gs}, V_{ds})$. The functional relationship becomes:

$i_{ds} = I_{ds}(V_{gs}, V_{ds}) * v_{ds} / V_{ds}$.

More than one [Series MOSFET] table is permitted, but it is simulator dependent how the data will be used. Each successive [Series MOSFET] table must have a different subparameter value for V_{ds} . The number of tables must not exceed 100. C_{comp} values are ignored for [Series MOSFET] models.

#32 Series MOSFET

[On]

[Series MOSFET]

$V_{ds} = 1.0$

Voltage	I (typ)	I (min)	I (max)	
5.0V	257.9m	153.3m	399.5m	Defines I_{ds} current as a func. of V_{gs} , for $V_{ds} = 1.0$
4.0V	203.0m	119.4m	317.3m	
3.0V	129.8m	74.7m	205.6m	
2.0V	31.2m	16.6m	51.0m	
1.0V	52.7p	46.7p	56.7p	
0.0V	0.0p	0.0p	0.0p	

|

Table 5 (cont.): V-I Behavioral Properties

Keyword	Syntax	Rules	Notes
Vol, Voh	Vol = output low, Voh = output high. Note 1*.	3Com spec. Not an IBIS spec	Note 18. Example #33
Technology	40 characters max*	3Com spec. Not an IBIS spec	Note 19. Example #34
[Pulldown]	Note 1*.	The V-I curve rules are straightforward, but lengthy.	Note 6, Example #35
[Pullup]			
[GND Clamp]			
[POWER Clamp]			

(Cont.)

* Assumed: Consistent with IBIS syntax.

Note 18

Most simulators will calculate time-of-flight results if provided with Vol and Voh for output buffers. IBIS avoids getting into timing type data and thus doesn't require these measurements. 3Com considers this an oversight and routinely request this data be supplied with IBIS models. Vol and Voh are routinely provided on supplier data sheets.

#33 Vol/Voh

```
Vinl = 0.8V          | output logic "low" DC voltage, if any
Vinh = 2.0V          | output logic "high" DC voltage, if any
```

Note 19

Most simulators can be set up to default to a signal model based on a particular type of technology (standard TTL, LVTTTL, etc.) and assigned pin use when a component specific IBIS model is not available or is not yet assigned to the part. The default model is most accurate when its technology type matches that of the component. Suppliers shall be expected to identify the technology type of their I/O buffers to facilitate this match up.

#34 Technology

Technology LVTTL

Note 6

In each of these sections, the first column contains the voltage value, and the three remaining columns hold the typical, minimum, and maximum current values. The four entries, Voltage, I(typ), I(min), and I(max) must be placed on a single line and must be separated by at least one white space or tab character.

All four columns are required under these keywords. However, data is only required in the typical column. If minimum and/or maximum current values are not available, the reserved word "NA" must be used. "NA" can be used for currents in the typical column, but numeric values MUST be specified for the first and last voltage points on any V/I curve. Each V/I curve must have at least 2, but not more than 100, voltage points.

The V/I curve of the [Pullup] and the [POWER Clamp] structures are 'Vcc relative', meaning that the voltage values are referenced to the Vcc pin. (Note: Under these keywords, all references to 'Vcc' refer to the voltage rail defined by the [Voltage range], [Pullup Reference], or [POWER Clamp Reference] keywords, as appropriate.) The voltages in the data tables are derived from the equation:

$$V_{table} = V_{cc} - V_{output}.$$

Therefore, for a 5 V component, -5 V in the table actually means 5 V above Vcc, which is +10 V with respect to ground; and 10 V means 10 V below Vcc, which is -5 V with respect to ground. Vcc-relative data is necessary to model a pull-up structure properly, since the output current of a pull-up structure depends on the voltage between the output and Vcc pins and not the voltage between the output and ground pins.

Note that the [GND Clamp] V/I curve can include quiescent input currents, or the currents of a 3-stated output, if so desired.

When tabulating data for ECL devices, the data in the pull-down table is measured with the output in the 'logic low' state. In other words, the data in the table represents the V/I characteristics of the output when the output is at the most negative of its two logic levels. Likewise, the data in the pull-up table is measured with the output in the 'logic one' state and represents the V/I characteristics when the output is at the most positive logic level.

Note that in BOTH of these cases, the data is referenced to the Vcc supply voltage, using the equation:

$$V_{table} = V_{cc} - V_{output}.$$

Monotonicity Requirements:

To be monotonic, the V/I table data must meet any one of the following 8 criteria:

- 1 - The CURRENT axis either increases or remains constant as the voltage axis is increased.
- 2 - The CURRENT axis either increases or remains constant as the voltage axis is decreased.
- 3 - The CURRENT axis either decreases or remains constant as the voltage axis is increased.
- 4 - The CURRENT axis either decreases or remains constant as the voltage axis is decreased.
- 5 - The VOLTAGE axis either increases or remains constant as the current axis is increased.
- 6 - The VOLTAGE axis either increases or remains constant as the current axis is decreased.
- 7 - The VOLTAGE axis either decreases or remains constant as the current axis is increased.
- 8 - The VOLTAGE axis either decreases or remains constant as the current axis is decreased.

An IBIS syntax checking program shall test for non-monotonic data and provide a maximum of one note per V/I table if non-monotonic data is found. For example:

"NOTE: Line 300, Pulldown V/I table for model DC040403 is non-monotonic! Most simulators will filter this data to remove the non-monotonic data."

It is also recognized that the data may be monotonic if currents from both the output stage and the clamp diode are added together as most simulators do. To limit the complexity of the IBIS Version 2.x and Version 3.x syntax checking programs, such programs will conduct monotonicity testing only on one V/I table at a time.

It is assumed that the simulator sums the clamp tables together with the appropriate [Pullup] or [Pulldown] table when a buffer is driving high or low, respectively. From this assumption and the nature of 3-statable buffers, it follows that the data in the clamping table sections are handled as constantly present tables and the [Pullup] and [Pulldown] tables are used only when needed in the simulation.

The clamp tables of an Input or I/O buffer can be measured directly with a curve tracer, with the I/O buffer 3-stated. However, sweeping enabled buffers results in tables that are the sum of the clamping tables and the output structures. Based on the assumption outlined above, the [Pullup] and [Pulldown] tables of an IBIS model must represent the difference of the 3-stated and the enabled buffer's tables. (Note that the resulting difference table can demonstrate a non-monotonic shape.) This requirement enables the simulator to sum the tables, without the danger of double counting, and arrive at an accurate model in both the 3-stated and enabled conditions.

Since in the case of a non 3-statable buffer, this difference table cannot be generated through lab measurements (because the clamping tables cannot be measured alone), the [Pullup] and [Pulldown] tables of an IBIS model can contain the sum of the clamping characteristics and the output structure. In this case, the clamping tables must contain all zeroes, or the keywords must be omitted.

#35 Pullup/Pulldown/POWER Clamp/GND Clamp

[Pullup]				Note: Vtable = Vcc - Voutput
Voltage	I (typ)	I (min)	I (max)	
-5.0V	32.0m	30.0m	35.0m	
-4.0V	31.0m	29.0m	33.0m	
.				
.				
0.0V	0.0m	0.0m	0.0m	
.				
.				
5.0V	-32.0m	-30.0m	-35.0m	
10.0V	-38.0m	-35.0m	-40.0m	
[Pulldown]				
Voltage	I (typ)	I (min)	I (max)	
-5.0V	-40.0m	-34.0m	-45.0m	
-4.0V	-39.0m	-33.0m	-43.0m	
.				
.				
0.0V	0.0m	0.0m	0.0m	
.				
.				
5.0V	40.0m	34.0m	45.0m	
10.0V	45.0m	40.0m	49.0m	
[POWER Clamp]				Note: Vtable = Vcc - Voutput
Voltage	I (typ)	I (min)	I (max)	
-5.0V	4450.0m	NA	NA	
-0.7V	95.0m	NA	NA	
-0.6V	23.0m	NA	NA	
-0.5V	2.4m	NA	NA	
-0.4V	0.0m	NA	NA	
0.0V	0.0m	NA	NA	
[GND Clamp]				
Voltage	I (typ)	I (min)	I (max)	

-5.0V	-3900.0m	-3800.0m	-4000.0m
-0.7V	-80.0m	-75.0m	-85.0m
-0.6V	-22.0m	-20.0m	-25.0m
-0.5V	-2.4m	-2.0m	-2.9m
-0.4V	0.0m	0.0m	0.0m
5.0V	0.0m	0.0m	0.0m

Table 5 (cont.): V-I Behavioral Properties

Keyword	Syntax	Rules	Notes
[Pullup Reference]	Note 1*.	Provide actual voltages (not percentages) in the typ, min, max format. This keyword also defines the voltage range over which the min and max dV/dt_r values are derived.	Example #36
[Pulldown Reference]		Ibid - This keyword, also defines the voltage range over which the typ, min, and max dV/dt_f values are derived.	
[GND Clamp Reference]		Provide actual voltages (not percentages) in the typ, min, max format. Power Supplies: It is intended that standard TTL and CMOS devices be specified using only the [Voltage Range] keyword. However, in cases where output characteristics of a device depend on more than a single supply and ground, or a pull-up, pull-down, or clamp structure is referenced to something other than the default supplies, use the additional 'reference' keywords.	
[POWER Clamp Reference]		Provide actual voltages (not percentages) in the typ, min, max format.	

(cont.)

*Assumed: Consistent with IBIS spec.

#36 Pullup/Pulldown/POWER Clamp/GND Clamp Reference

variable	typ	min	max
[Pullup Reference]	5.0V	4.5V	5.5V
variable	typ	min	max
[Pulldown Reference]	0V	0V	0V
variable	typ	min	max
[POWER Clamp Reference]	5.0V	4.5V	5.5V
variable	typ	min	max
[GND Clamp Reference]	0V	0V	0V

Table 5 (cont.): V-I Properties

Keyword	Syntax	Rules	Notes
[Model Selector]	Used to pick a [Model] from a list of [Model]s for a pin which uses a programmable buffer. 20 characters max. The section under the [Model Selector] keyword must have 2 fields. The 2 fields must be separated by at least 1 space.	A .ibs file must contain enough [Model Selector] keywords to cover all model selector names specified in the [Pin] and [Series Pin Mapping] keywords.	Note 20. Example #37

Note 20

A programmable buffer must have an individual [Model] section for each one of its modes used in the .ibs file. The names of these [Model]s must be unique and can be listed under the [Model Selector] keyword and/or pin list. The name of the [Model Selector] keyword must match the corresponding model name listed under the [Pin] or [Series Pin Mapping] keyword.

The first field lists the [Model] name (up to 20 characters long). The second field contains a short description of the [Model] shown in the first field. The contents and format of this description is not standardized, however it shall be limited in length so that none of the descriptions exceed the 80-character length of the line that it started on. The purpose of the descriptions is to aid the user of the simulator tool in making intelligent buffer mode selections and it can be used by the simulator tool in a user interface dialog box as the basis of an interactive buffer selection mechanism.

The first entry under the [Model Selector] keyword shall be considered the default by the simulator tool for all those pins which call this [Model Selector].

The operation of this selection mechanism implies that a group of pins which use the same programmable buffer (i.e. model selector name) will be switched together from one [Model] to another. Therefore, if two groups of pins, for example an address bus and a data bus, use the same programmable buffer, and the user must have the capability to configure them independently, one can use two [Model Selector] keywords with unique names and the same list of [Model] keywords; however, the usage of the [Model Selector] is not limited to these examples. Many other combinations are possible.

*Assumed: Consistent with IBIS spec.

#37 Model Selector

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
1	RAS0#	Progbuffer1	200.0m	5.0nH	2.0pF
2	EN1#	Input1	NA	6.3nH	NA
3	A0	3-state			
4	D0	Progbuffer2			
5	D1	Progbuffer2	320.0m	3.1nH	2.2pF
6	D2	Progbuffer2			
7	RD#	Input2	310.0m	3.0nH	2.0pF
.					
.					
.					
18	Vcc3	POWER			
	[Model Selector]	Progbuffer1			
OUT_2	2 mA buffer without slew rate control				
OUT_4	4 mA buffer without slew rate control				
OUT_6	6 mA buffer without slew rate control				
OUT_4S	4 mA buffer with slew rate control				
OUT_6S	6 mA buffer with slew rate control				
	[Model Selector]	Progbuffer2			
OUT_2	2 mA buffer without slew rate control				
OUT_6	6 mA buffer without slew rate control				
OUT_6S	6 mA buffer with slew rate control				
OUT_8S	8 mA buffer with slew rate control				
OUT_10S	10 mA buffer with slew rate control				

Table 5 (cont.): V-I Properties

Keyword	Syntax	Rules	Notes
[Model Spec]	Must follow all other sub parameters under the [Model] keyword	Defines 4 columns under which keyword subparameters are defined	Note 34. Example #38
	Vinh input Vt high: Note 1*		
	Vinl input Vt low Note 1*.		
	Vinh+ hysteresis Vt+ high max: Note 1*		
	Vinh- hysteresis Vt+ high min: Note 1*		
	Vinl+ hysteresis Vt- low max: Note 1*		
	Vinl- hysteresis Vt- low min: Note 1*		
	S_overshoot_high static overshoot high voltage note 1*		
	S_overshoot_low static overshoot low voltage note 1*		
	D_overshoot_high dynamic overshoot hi volt. note 1*		
	D_overshoot_low dynamic overshoot low volt. note 1*		
	D_overshoot_time dynamic overshoot time note 1*		
	Pulse_high pulse immunity hi volt. note 1*		
	Pulse_low pulse immunity low volt. note 1*		
	Pulse_time pulse immunity time note 1*		
	Vmeas Volt. for timing measure note 1*		

(cont.)

Note 34

For each subparameter contained in the first column, the remaining three hold its typical, minimum and maximum values. The entries of typical, minimum and maximum must be placed on a single line and must be separated by at least one white space or tab character. All four columns are required under the [Model Spec] keyword. However, data is required only in the typical column. If minimum and/or maximum values are not available, the reserved word "NA" must be used indicating the typical value by default.

The minimum and maximum values are used for specifications subparameter values that may track the min and max operation conditions of the [Model]. Usually it is related to the Voltage Range settings. Unless noted below, each subparameter does not require having any other subparameter.

Vinh, Vinl rules:

The threshold subparameter lines provide additional min and max column values, if needed. The typ column values are still required and would be expected to override the Vinh and Vinl subparameter values specified elsewhere. Note: the syntax rule that require inserting Vinh and Vinl under models remains unchanged even if the values are defined under the [Model Spec] keyword.

To mimic a hysteresis effect, the values of Vinh and Vinl may be interchanged such that the Vinl value is larger than the Vinh value. However, simulators may process this information differently or report an error.

Vinh+, Vinh-, Vinl+, Vinl- rules:

The four hysteresis subparameters must all be defined before the hysteresis threshold rules become effective. Otherwise the standard threshold subparameters remain in effect. The hysteresis thresholds shall be at the Vinh+ and Vinh- values for a low-to-high transition, and at the Vinl+ and Vinl- values for a high-to-low transition.

S_overshoot_high, S_overshoot_low rules:

The static overshoot subparameters provide the voltage values for which the model is no longer guaranteed to function correctly.

D_overshoot_high, D_overshoot_low, D_overshoot_time rules:

The dynamic overshoot values provide a time window during which the overshoot may exceed the static overshoot limits but be below the dynamic overshoot limits. D_overshoot_time is required for dynamic overshoot testing. In addition, if D_overshoot_high is specified, then S_overshoot_high is necessary for testing beyond the static limit. Similarly, if D_overshoot_low is specified, then S_overshoot_low is necessary for testing beyond the static limit.

Pulse_high, Pulse_low, Pulse_time rules:

The pulse immunity values provide a time window during which a rising pulse may exceed the nearest threshold value but be below the pulse voltage value and still not cause the input to switch. Pulse_time is required for pulse immunity testing. A rising response is tested only if Pulse_high is specified. Similarly, a falling response is tested only if Pulse_low is specified. The rising response may exceed the

Vinl value, but remain below the Pulse_high value.

Similarly, the falling response may drop below the Vinh value, but remain above the Pulse_low value. In either case the input is regarded as immune to switching if the responses are within these extended windows. If the hysteresis thresholds are defined, then the rising response shall use Vinh- as the reference voltage, and the falling response shall use Vinl+ as the reference voltage.

Vmeas rules:

The Vmeas values under the [Model Spec] keyword override the Vmeas entry elsewhere.

#38 Model Spec

[Model Spec]				
Subparameter	typ	min	max	
Thresholds				
Vinh	3.5	3.15	3.85	70% of Vcc
Vinl	1.5	1.35	1.65	30% of Vcc
Vinh	3.835	3.335	4.335	Offset from Vcc
Vinl	3.525	3.025	4.025	for PECL
Hysteresis				
Vinh+	2.0	NA	NA	Overrides the
Vinh-	1.6	NA	NA	thresholds
Vinl+	1.1	NA	NA	
Vinl-	0.6	NA	NA	All 4 required
Overshoot				
S_overshoot_high	5.5	5.0	6.0	Static overshoot
S_overshoot_low	-0.5	NA	NA	
D_overshoot_high	6.0	5.5	6.5	Dynamic overshoot
D_overshoot_low	-1.0	-1.0	-1.0	req D_overshoot
				_time & static
D_overshoot_time	20n	20n	20n	overshoot
Pulse Immunity				
Pulse_high	3V	NA	NA	Pulse immunity
Pulse_low	0	NA	NA	requires
Pulse_time	3n	NA	NA	Pulse_time
Timing Thresholds				
Vmeas	3.68	3.18	4.68	A 5 volt PECL
				example

Table 5 (cont.): V-I Properties

Keyword	Syntax	Rules	Notes
[Add Submodel]	Invoked within a model. 1 st column contains the <i>submodel_name</i> . 2 nd column contains the submodel <i>mode</i>	References a submodel to be added to an existing model	Note 21. Example #39
	submodel_name 20 characters max	Only allows: Dynamic_clamp or Bus_hold	
	mode	Only allows: Driving, Non-Driving or All	
[Submodel]		Used to define a submodel and its attributes	Note 27. Examples #40 & #41
	Submodel_type	Must be Dynamic_clamp or Bus_hold	
[Submodel Spec]	To be used only with [Submodels]	Defines 4 columns under which specs and information subparameters are defined for submodels	Note 28. Examples #41 & #42
	V_trigger_r Rising edge trigger volt. Note 1*		
	V_trigger_f Falling edge trigger volt. Note 1*		
	Off_delay Turnoff delay from V_trigger_r or V_trigger_f. Note 1*		

(Cont.)

Note 21

The [Add Submodel] keyword is invoked within a model to add the functionality that is contained in the submodel or list of submodels in each line that follows. The first column contains the submodel name. The second column contains a submodel mode under which the submodel is used.

If the top-level model type is one of the I/O or 3-state models, the submodel mode may be Driving, Non-Driving, or All. For example, if the submodel mode is Non-Driving, then the submodel is used only in the high-Z state of a 3-state model. Set the submodel mode to All if the submodel is to be used for all modes of operation.

The submodel mode cannot conflict with the top-level model type. For example, if the top-level model type is an Open or Output type, the submodel mode cannot be set to Non-Driving. Similarly, if the top-level model type is Input, the submodel mode cannot be set to Driving.

The [Add Submodel] keyword is not defined for Series or, Series_switch model types. Refer to the Add Submodel Description section in this document for the descriptions of available submodels.

#39 Add Submodel

[Add Submodel]		
Submodel_name	Mode	
Bus_Hold_1	Non-Driving	Adds electrical character. of
		[Submodel] Bus_Hold_1 for receiver or
		high-Z mode only
Dynamic_clamp_1	All	Adds the Dynmanic_clamp_1 model for
		all modes of operation

Note 27

Each submodel must begin with the keyword [Submodel]. The submodel name must match the one that is listed under the [Add Submodel] keyword. A .ibs file must contain enough [Submodel] keywords to cover all of the model names specified under the [Add Submodel] keyword.

The C_comp subparameter is not permitted under the [Submodel] keyword. The total effective die capacitance including the submodel contributions are provided in the top-level model.

The following list of keywords that are defined under the [Model] keyword can be used under [Submodel]:
[Pulldown], [Pullup], [GND Clamp], [POWER Clamp], [Ramp], [Rising Waveform], and [Falling Waveform].

The following list of additional keywords can be used:
[Submodel Spec], [GND Pulse Table], and [POWER Pulse Table].

#40 Submodel

[Submodel]	Dynamic_clamp1
Submodel_type	Dynamic_clamp

Note 28

For each subparameter contained in the first column, the remaining three hold its typical, minimum and maximum values. The entries of typical, minimum and maximum must be placed on a single line and must be separated by at least one white space or tab character. All four columns are required under the [Submodel Spec] keyword. However, data is required only in the typical column. If minimum and/or maximum values are not available, the reserved word "NA" must be used to indicate the typical value by default.

The values in the minimum and maximum columns usually correspond to the values in the same columns for the inherited top-level voltage range or reference voltages in the top-level model. The V_trigger_r and V_trigger_f subparameters should hold values in the minimum and maximum columns that correspond to the voltage range or reference voltages of the top-level model. The Off_delay subparameter, however, is an exception to this rule because in some cases it may be completely or partially independent from supply voltages and/or manufacturing process variations. Therefore the minimum and maximum entries for the Off_delay subparameter should be ordered simply by their magnitude.

Unless noted, each [Submodel Spec] subparameter is independent of any other subparameter.

V_trigger_r, V_trigger_f rules:

The voltage trigger values for the rising and falling edges provide the starting time when an action is initiated.

Off_delay rules:

The functionality of the Off_delay subparameter is to provide an additional time related mechanism to turn off circuit elements.

#41 Complete Bus Hold & Timed Latch Examples

```
|
| Complete Bus Hold Model Example:
|
[Submodel]      Bus_hold_1
Submodel_type    Bus_hold
|
[Submodel Spec]
|   Subparameter    typ        min        max
|
V_trigger_f      1.3        1.2        1.4   | Falling edge trigger
V_trigger_r      3.1        2.6        4.6   | Rising edge trigger
|
|               typ        min        max
| [Voltage Range] 5.0        4.5        5.5
| Note, the actual voltage range and reference volt. are inherited from
| the top-level model.
|
[Pulldown]
```



```

|
-5V      -100uA    -80uA    -120uA
-1V      -30uA     -25uA    -40uA
0V        0         0        0
1V        30uA     25uA     40uA
3V        50uA     45uA     50uA
5V       100uA     80uA     120uA
10v      120uA     90uA     150uA
|
[Pullup]
|
-5V       100uA     80uA     120uA
-1V       30uA     25uA     40uA
0V         0         0         0
1V       -30uA    -25uA    -40uA
3V       -50uA    -45uA    -50uA
5V      -100uA    -80uA    -120uA
10v     -120uA    -90uA    -150uA
|
|-----
|
[Ramp]
|
|                                     typ          min          max
dV/dt_r          2.0/0.50n          2.0/0.75n          2.0/0.35n
dV/dt_f          2.0/0.50n          2.0/0.75n          2.0/0.35n
R_load = 500
|
|
| Complete Pullup Timed Latch Example:
|
[Submodel]      Timed_pullup_latch
Submodel_type    Bus_hold
|
[Submodel Spec]
| Subparameter    typ          min          max
|
V_trigger_r      3.1          2.6          4.6 | Rising edge trigger
|                                     | Values could be out
|                                     | of range to disable the
|                                     | trigger
V_trigger_f      1.3          1.2          1.4 | Falling edge trigger
Off_delay        3n          5n          2n  | Delay to turn off the
| pullup table
|
| Note that if the input signal goes above the V_trigger_r value, the
| pulldown structure will turn off even if the timer didn't expire yet.
|
|                                     typ          min          max
| [Voltage Range] 5.0          4.5          5.5
| Note, the actual voltage range and ref. voltages are inherited from
| the top-level model.
|
[Pulldown]
|
-5V      -100uA    -80uA    -120uA
-1V      -30uA     -25uA    -40uA

```

0V	0	0	0
1V	30uA	25uA	40uA
3V	50uA	45uA	50uA
5V	100uA	80uA	120uA
10v	120uA	90uA	150uA

|

| [Pullup] table is omitted to signal Open_source functionality

|

|-----

|

[Ramp]

	typ	min	max
dV/dt_r	2.0/0.50n	2.0/0.75n	2.0/0.35n
dV/dt_f	2.0/0.50n	2.0/0.75n	2.0/0.35n

R_load = 500

|

#42 Submodel Spec

| Dynamic Clamp Example:

|

[Submodel Spec]

Subparameter	typ	min	max	
--------------	-----	-----	-----	--

|

V_trigger_r	3.6	2.9	4.3	Starts pwr pulse table
V_trigger_f	1.4	1.2	1.6	Starts gnd pulse table

|

| Bus Hold Example:

|

[Submodel Spec]

Subparameter	p	min	max	
--------------	---	-----	-----	--

V_trigger_r	3.1	2.4	3.7	Starts low to high bus hold transition
V_trigger_f	1.8	1.6	2.0	Starts high to low bus hold transition

|

| Bus_hold app with pullup structure triggered on and then clocked off:

|

[Submodel Spec]

Subparameter	typ	min	max	
--------------	-----	-----	-----	--

V_trigger_r	3.1	2.4	3.7	Low to high transition triggers the turn on
V_trigger_f	-10.0	-10.0	-10.0	Not used, so trigger voltages are set out of range
Off_delay	5n	6n	4n	Time from rising edge trigger at which the pullup turned off

|

```

| Ex. of Dynamic_clamp Model with both dynamic GND and POWER clamps:
|
| [Submodel]          Dynamic_Clamp_1
| Submodel_type       Dynamic_clamp
|
| [Submodel Spec]
|   Subparameter      typ          min          max
|
| V_trigger_f          1.4          1.2          1.6 | Falling edge trigger
| V_trigger_r          3.6          2.9          4.3 | Rising edge trigger
|
|                               typ          min          max
| [Voltage Range]      5.0          4.5          5.5
| Note, the actual voltage range and ref voltages are inherited from
| the top-level model.

```

Table 5 (cont.): V-I Properties

Keyword	Syntax	Rules	Notes
[GND Pulse Table]	Note 1*.	Used to specify the offset voltage Vs time of [GND Clamp] and [POWER Clamp] tables within submodels. Note 29	Example #43
[POWER Pulse Table]			Example #44
[TTgnd]	Note 1*.	Transit time parameters used to estimate TT capacitances and tables for GND & POWER clamp tables	Example #45
[TTpower]			

*Assumed: Consistent with IBIS spec.

Note 29

Each [GND Pulse Table] and [POWER Pulse Table] keyword introduces a table of time versus vs. points that describe the shape of an offset voltage from the [GND Clamp Reference] voltage (or default ground) or the [POWER Clamp Reference] voltage (or default [Voltage Range] voltage). Note, these voltage values are inherited from the top-level model.

The table itself consists of one column of time points, then three columns of voltage points in the standard typ, min, and max format. The four entries must be placed on a single line and must be separated by at least one white space or tab character. All four columns are required. However, data is only required in the typical column. If minimum or maximum data is not available, use the reserved word "NA". Time values must increase as one parses down the table. The waveform table can contain of maximum of 100 data points.

Each table must contain at least two entries. Thus, numerical values are required for the first and last entries of any column containing numerical data.

The voltage entries in both the [Gnd Pulse Table] and [POWER Pulse Table] tables are directly measured offsets. At each instance, the [Gnd Pulse Table] voltage is ADDED to the [GND Clamp] table voltages to provide the shifted table voltages. At each instance, the [POWER Pulse Table] voltage is SUBTRACTED (because of polarity conventions) from the [POWER Clamp] table voltages to provide the shifted table voltages. Only one [GND Pulse Table] and one [POWER Pulse Table] are allowed per model.

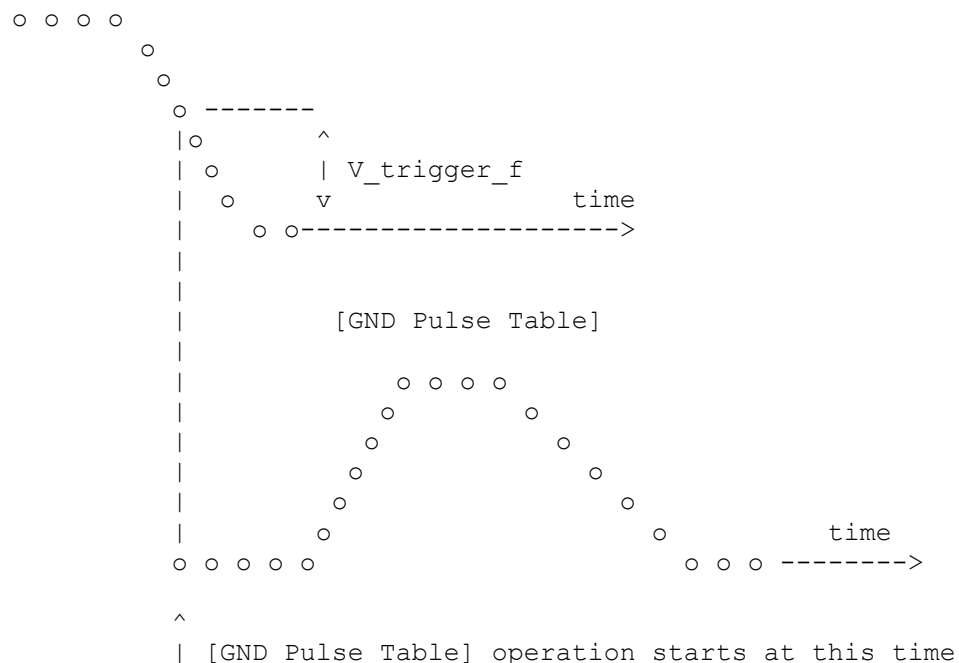
The [GND Pulse Table] and [POWER Pulse Table] interact with [Submodel Spec] subparameters V_trigger_f and V_trigger_r. Several modes of operation exist based on whether a pulse table and its corresponding trigger subparameter are given. These modes are classified as triggered and static.

Triggered Mode:

For triggered mode a pulse table must exist and include the entire waveform; i.e., the first entry (or entries) in a voltage column must be equal to the last entry. Also, a corresponding [Submodel Spec] V_trigger_* subparameter must exist. The triggered interaction is described:

The V_trigger_f subparameter under [Submodel Spec] is used to detect when the falling edge waveform at the die passes the trigger voltage. At that time the [Gnd Pulse Table] operation starts. Similarly, the V_trigger_r subparameter is used to detect when the rising edge waveform at the die passes the trigger voltage. At that time [POWER Pulse Table] operation starts. The [GND Pulse Table] dependency is shown below:

Waveform at Die



The V_trigger_r and [POWER Pulse Table] operate in a similar manner. When the V_trigger_r voltage value is reached on the rising edge, the [POWER Pulse Table] is started. Normally the offset voltage entries in the [POWER Pulse Table] are negative.

Static Mode:

When the [GND Pulse Table] keyword does not exist, but the added model [GND Clamp] table does exist, the added model [GND Clamp] is used directly. Similarly, when the [POWER Pulse Table] keyword does not exist, but the added model [POWER Clamp] table does exist, the added model [POWER Clamp] is used directly. This mode provides additional fixed clamping to an I/O_* buffer or a 3-state buffer when it is used as a driver.

#43 GND Pulse Table

[GND Pulse Table]			GND Clamp offset table	
Time	V (typ)	V (min)	V (max)	
0	0	0	0	
1e-9	0	0	0	
2e-9	0.9	0.8	1.0	
10e-9	0.9	0.8	1.0	
11e-9	0	0	0	
[GND Clamp]			Table to be offset	
Voltage	I (typ)	I (min)	I (max)	
-5.000	-3.300e+01	-3.000e+01	-3.500e+01	
-4.000	-2.300e+01	-2.200e+01	-2.400e+01	
-3.000	-1.300e+01	-1.200e+01	-1.400e+01	
-2.000	-3.000e+00	-2.300e+00	-3.700e+00	
-1.900	-2.100e+00	-1.500e+00	-2.800e+00	
-1.800	-1.300e+00	-8.600e-01	-1.900e+00	
-1.700	-6.800e-01	-4.000e-01	-1.100e+00	
-1.600	-2.800e-01	-1.800e-01	-5.100e-01	
-1.500	-1.200e-01	-9.800e-02	-1.800e-01	
-1.400	-7.500e-02	-7.100e-02	-8.300e-02	
-1.300	-5.750e-02	-5.700e-02	-5.900e-02	
-1.200	-4.600e-02	-4.650e-02	-4.550e-02	
-1.100	-3.550e-02	-3.700e-02	-3.450e-02	
-1.000	-2.650e-02	-2.850e-02	-2.500e-02	
-0.900	-1.850e-02	-2.100e-02	-1.650e-02	
-0.800	-1.200e-02	-1.400e-02	-9.750e-03	
-0.700	-6.700e-03	-8.800e-03	-4.700e-03	
-0.600	-3.000e-03	-4.650e-03	-1.600e-03	
-0.500	-9.450e-04	-1.950e-03	-3.650e-04	
-0.400	-5.700e-05	-2.700e-04	-5.550e-06	
-0.300	-1.200e-06	-1.200e-05	-5.500e-08	
-0.200	-3.000e-08	-5.000e-07	0.000e+00	
-0.100	0.000e+00	0.000e+00	0.000e+00	
0.000	0.000e+00	0.000e+00	0.000e+00	
5.000	0.000e+00	0.000e+00	0.000e+00	

#44 POWER Pulse Table

[POWER Pulse Table]		POWER Clamp offset table	
Time	V(typ)	V(min)	V(max)
0	0	0	0
1e-9	0	0	0
2e-9	-0.9	-1.0	-0.8
10e-9	-0.9	-1.0	-0.8
11e-9	0	0	0
[POWER Clamp]		Table to be offset	
Voltage	I (typ)	I (min)	I (max)
-5.000	1.150e+01	1.100e+01	1.150e+01
-4.000	7.800e+00	7.500e+00	8.150e+00
-3.000	4.350e+00	4.100e+00	4.700e+00
-2.000	1.100e+00	8.750e-01	1.300e+00
-1.900	8.000e-01	6.050e-01	1.000e+00
-1.800	5.300e-01	3.700e-01	7.250e-01
-1.700	2.900e-01	1.800e-01	4.500e-01
-1.600	1.200e-01	6.850e-02	2.200e-01
-1.500	3.650e-02	2.400e-02	6.900e-02
-1.400	1.200e-02	1.100e-02	1.600e-02
-1.300	6.300e-03	6.650e-03	6.100e-03
-1.200	4.200e-03	4.750e-03	3.650e-03
-1.100	2.900e-03	3.500e-03	2.350e-03
-1.000	1.900e-03	2.450e-03	1.400e-03
-0.900	1.150e-03	1.600e-03	7.100e-04
-0.800	5.500e-04	9.150e-04	2.600e-04
-0.700	1.200e-04	4.400e-04	5.600e-05
-0.600	5.400e-05	1.550e-04	1.200e-05
-0.500	1.350e-05	5.400e-05	1.300e-06
-0.400	8.650e-07	7.450e-06	4.950e-08
-0.300	6.250e-08	7.550e-07	0.000e+00
-0.200	0.000e+00	8.400e-08	0.000e+00
-0.100	0.000e+00	0.000e-08	0.000e+00
0.000	0.000e+00	0.000e+00	0.000e+00

#45 TTgnd/TTpower

variable	TT (typ)	TT (min)	TT (max)
[TTgnd]	10n	12n	9n
[TTpower]	12n	NA	NA

Table 6: V-T Behavioral Properties

Keyword	Syntax	Rules	Notes
[Ramp]	Note 1* applies to all sub parameters	The ramp rate does not include packaging but does include the effects of the C_comp parameter.	Note 8, Example #46
	dV/dt_r		
	dV/dt_f		
	R_load		
	Vmeas	Test fixture parameters	
	Cref		
	Rref		
	Vref		
[Rising Waveform] & [Falling Waveform]	Note 1* applies to all sub parameters		Note 9, Example #47
	R_fixture		
	C_fixture		
	L_fixture		
	V_fixture		
	V_fixture_min		
	V_fixture_max		
	R_dut		
	C_dut		
	L_dut		

Note 8

The rise and fall time is defined as the time it takes the output to go from 20% to 80% of its final value. The ramp rate is defined as:

$$\text{ramp rate} = \frac{\text{dV}}{\text{dt}} = \frac{\text{20\% to 80\% voltage swing}}{\text{Time it takes to swing the above voltage}}$$

The ramp rate must be specified as an explicit fraction and must not be reduced. The [Ramp] values can use "NA" for the min and max values only. The R_load subparameter is optional if the preferred 50 ohm load is used. The R_load sub-parameter is required if a non-standard load is used.

#46 Ramp

```
[Ramp]
| variable      typ          min          max
dV/dt_r        2.20/1.06n    1.92/1.28n    2.49/650p
dV/dt_f        2.46/1.21n    2.21/1.54n    2.70/770p
R_load = 300ohms
|
```

Note 9

Each [Rising Waveform] and [Falling Waveform] keyword introduces a table of time vs. voltage points that describe the shape of an output waveform. These time/voltage points are taken under the conditions specified in the R/L/C/V_fixture and R/L/C_dut subparameters. The table itself consists of one column of time points, then three columns of voltage points in the standard typ, min, and max format. The four entries must be placed on a single line and must be separated by at least one white space or tab character. All four columns are required. However, data is only required in the typical column. If minimum or maximum data is not available, use the reserved word "NA". The first value in the time column need not be '0'. Time values must increase as one parses down the table. The waveform table can contain a maximum of 100 data points. A maximum of 100 waveform tables are allowed per model.

Note that for backwards compatibility, the existing [Ramp] keyword is still required. The data in the waveform table is taken with the effects of the C_comp parameter included.

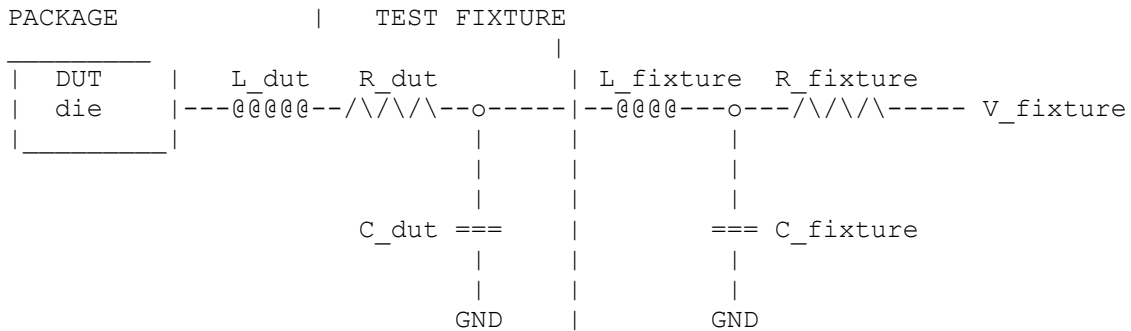
A waveform table must include the entire waveform; i.e., the first entry (or entries) in a voltage column must be the DC voltage of the output before switching and the last entry (or entries) of the column must be the final DC value of the output after switching.

Each table must contain at least two entries. Thus, numerical values are required for the first and last entries of any column containing numerical data.

A [Model] specification can contain more than one rising edge or falling edge waveform table. However, each new table must begin with the appropriate keyword and sub-parameter list as shown below. If more than one rising or falling edge waveform table is present, then the data in each of the respective tables must be time correlated. In other words, the rising (falling) edge data in each of the rising (falling) edge waveform tables must be entered with respect to a common reference point on the input stimulus waveform.

The 'fixture' subparameters specify the loading conditions under which the waveform is taken. The R_dut, C_dut, and L_dut subparameters are analogous to the package parameters R_pkg, C_pkg, and L_pkg and are used if the waveform includes the effects of pin inductance/capacitance. The diagram below

shows the interconnection of these elements.



NOTE: The use of L_dut, R_dut, and C_dut is strongly discouraged in developing Waveform data from simulation models. Some simulators may ignore these parameters because they may introduce numerical time constant artifacts.

Only the R_fixture and V_fixture subparameters are required, the rest of the subparameters are optional. If a subparameter is not used, its value defaults to zero. The subparameters must appear in the text after the keyword and before the first row of the waveform table.

V_fixture defines the voltage for typ, min, and max supply conditions. However, when the fixture voltage is related to the power supply voltages, then the subparameters V_fixture_min and V_fixture_max can be used to further specify the fixture voltage for min and max supply voltages.

NOTE: Test fixtures with R_fixture and V_fixture, V_fixture_min, and V_fixture_max only are strongly encouraged because they provide the BEST set of data needed to produce the best model for simulation. C_fixture and L_fixture can be used to produce waveforms which describe the typical test case setups for reference.

All tables assume that the die capacitance is included. Potential numerical problems associated with processing the data using the effective C_comp for effective die capacitance may be handled differently among simulators.

#47 Rising/Falling Waveform

```
[Rising Waveform]
R_fixture = 50
V_fixture = 0.0
| C_fixture = 50p | These are shown, but are generally not recommended
| L_fixture = 2n
| C_dut = 7p
| R_dut = 1m
| L_dut = 1n
```

Time	V(typ)	V(min)	V(max)
0.0000S	25.2100mV	15.2200mV	43.5700mV
0.2000nS	2.3325mV	-8.5090mV	23.4150mV
0.4000nS	0.1484V	15.9375mV	0.3944V
0.6000nS	0.7799V	0.2673V	1.3400V
0.8000nS	1.2960V	0.6042V	1.9490V
1.0000nS	1.6603V	0.9256V	2.4233V
1.2000nS	1.9460V	1.2050V	2.8130V
1.4000nS	2.1285V	1.3725V	3.0095V
1.6000nS	2.3415V	1.5560V	3.1265V
1.8000nS	2.5135V	1.7015V	3.1600V
2.0000nS	2.6460V	1.8085V	3.1695V
...			
10.0000nS	2.7780V	2.3600V	3.1670V
[Falling Waveform]			
R_fixture = 50			
V_fixture = 5.5			
V_fixture_min = 4.5			
V_fixture_max = 5.5			
Time	V(typ)	V(min)	V(max)
0.0000S	5.0000V	4.5000V	5.5000V
0.2000nS	4.7470V	4.4695V	4.8815V
0.4000nS	3.9030V	4.0955V	3.5355V
0.6000nS	2.7313V	3.4533V	1.7770V
0.8000nS	1.8150V	2.8570V	0.8629V
1.0000nS	1.1697V	2.3270V	0.5364V
1.2000nS	0.7539V	1.8470V	0.4524V
1.4000nS	0.5905V	1.5430V	0.4368V
1.6000nS	0.4923V	1.2290V	0.4266V
1.8000nS	0.4639V	0.9906V	0.4207V
2.0000nS	0.4489V	0.8349V	0.4169V
...			
10.0000nS	0.3950V	0.4935V	0.3841V

Table 6 (cont.): V-T Properties

Keyword	Syntax	Rules	Notes
[Driver Schedule]	Establishes a hierarchical order. Place under [Model] which then acts as the top level model. Consists of 5 columns.	Describes relative switching sequence for referenced model to produce a multi-stage driver	Note 22. Example #48
	Rise_on_dly Note 1*	Driver scheduling can markedly affect the V-T characteristics of the I/O buffer.	
	Rise_off_dly Note 1*		
	Fall_on_dly Note 1*		
	Fall_off_dly Note 1*		

Note 22

Scheduled models are referenced from the top-level [Model] by the [Driver Schedule] keyword.

The [Driver Schedule] table consists of five columns. The first column contains the model names of other models that exists in the .libs file. The remaining four columns describe delays: Rise_on_dly, Rise_off_dly, Fall_on_dly, and Fall_off_dly. All values are referenced to 0 seconds for the start of the rising transition and 0 seconds for the start of the falling transition. All delays must be equal to or greater than 0.

The Rise_on_dly entry gives the beginning of the low-to-high transition. The Rise_off_dly entry may be given to end the low-to-high transition and initiate a high-to-low transition during the rising cycle. Similarly, the Fall_on_dly gives the beginning of the high-to-low transition. The Fall_off_dly may be given to end the high-to-low transition and initiate a low-to-high transition.

Use 'NA' when no transition is applicable. For each model, the transition sequence must be complete, i.e., it must start and end at the same state.

Only the [Pullup] and [Pulldown] tables and transition data [Ramp] or [Rising Waveform] and [Falling Waveform] data are used from each model that is referenced. The [Model] keyword provides the specification information, [GND Clamp] and [POWER Clamp], and C_comp, regardless of information contained in the referenced models.

It is recommended that a "golden waveform" for the device consisting of a [Rising Waveform] table and a [Falling Waveform] table be supplied under the [Model] keyword to serve as a reference for validation.

No [Driver Schedule] may reference a model which itself has within it a [Driver Schedule] table keyword.

The added models typically consist of `Open_sink` (`Open_drain`) or `Open_source` models to provide sequentially increased drive strengths. The added drive may be removed within the same transition for a momentary boost or during the opposite transition.

The syntax also allows for reducing the drive strength.

Note that the `Rise_on_dly`, `Rise_off_dly`, `Fall_on_dly`, `Fall_off_dly` parameters are single value parameters, so typical, minimum and maximum conditions cannot be described with them directly. In order to account for those effects, one can refer to the fastest waveform table with the delay number and then insert an appropriate amount of horizontal lead in section in those waveforms which need more delay.

Note: In a future release, the [Driver Schedule] keyword may be replaced by a newer method of specification that is consistent with some other planned extensions. However, the [Driver Schedule] syntax will continue to be supported.

#48 Driver Schedule

[Driver Schedule]				
Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
MODEL_OUT	0.0ns	NA	0.0ns	NA
Examples of added multi-staged transitions				
M_O_SOURCE1	0.5ns	NA	0.5ns	NA
	low (high-Z) to high		high to low (high-Z)	
M_O_SOURCE2	0.5n	1.5n	NA	NA
	low to high to low		low (high-Z)	
M_O_DRAIN1	1.0n	NA	1.5n	NA
	low to high (high-Z)		high (high-Z) to low	
M_O_DRAIN2	NA	NA	1.5n	2.0n
	high (high-Z)		high to low to high	

Table 7: Board Properties

Keyword	Syntax	Rules	Notes
[Begin Board Description]	File is stand-alone. <u>File name</u> is 8 characters max plus .ebd extension. Conforms to the rules general syntax rules of IBIS. Description field is 40 characters max.	Begins electrical board description file. File describes connections between the board pins and its components on the board.	Note 30. Example #49
[Manufacturer]	40 characters max. Can contain blank characters.	The maker of the board level component	Example #6
[Number of Pins]	Tells parser number of pins.	Pins are any externally accessible electrical connect. Simulator must allow 1000 pins minimum.	Example #15

(cont.)

Note 30

A fundamental assumption regarding the electrical board description is that the inductance and capacitance parameters listed in the file are derived with respect to well-defined reference plane(s) within the board. Also, this current description does not allow one to describe electrical (inductive or capacitive) coupling between paths. It is recommended that if coupling is an issue, then an electrical description be extracted from the physical parameters of the board.

What is, and is not, included in an Electrical Board Description is defined by its boundaries. For the definition of the boundaries, see the Description section under the [Path Description] Keyword.

The keyword is followed by the name of the board level component. If the .ebd file contains more than one [Begin Board Description] keyword, then each name must be unique. Blank characters are allowed. For every [Begin Board Description] keyword there must be a matching [End Board Description] keyword.

#49 Begin Board Description

```
[Begin Board Description] 16Meg X 8 SIMM Module
|
```

Table 7 (cont.): Board Properties

Keyword	Syntax	Rules	Notes
[Pin List]	Must follow [Number of Pins]. Pin names are 8 ASCII characters max.	Names of accessible pins including power and ground	Note 31. Example #50
[Path Description]	Each pin to node connect is divided into 1 or more cascaded sections, where each section is described in terms of its L/R/C per unit length. The Fork and Endfork subparameters allow the path to branch to multiple nodes, or another pin. Path descriptions required for each pin whose signal name is not "GND", "POWER" or "NC".	Describes connections from externally accessible pins and other pins or pins of ICs on board.	Note 32. Example #51
	Len		
	L, R, C Note 1*		
	Fork		
	Endfork		
	Pin		
	Node		

(cont.)

Note 31

Following the [Pin List] keyword are two columns. The first column lists the pin name while the second lists the data book name of the signal connected to that pin. There must be as many pin_name/signal_name rows as there are pins given by the preceding [Number Of Pins] keyword. Pin names must be the alphanumeric external pin names of the part. Any pin associated with a signal name that begins with "GND" or "POWER" will be interpreted as connecting to the boards ground or power plane.

In addition, NC is a legal signal name and indicates that the Pin is a 'no connect'. As per the IBIS standard "GND", "POWER" and "NC" are case insensitive.

#50 Pin List

```
| A SIMM Board Example
|
[Pin List]  signal_name
A1          GND
A2          data1
A3          data2
A4          POWER5      | this pin connects to 5v
A5          NC          | a no connect pin
| .
| .
A22         POWER3.3    | this pin connects to 3.3v
B1          casa
| .
| .
|etc.
```

Note 32

Board Description and IC Boundaries:

In any system, each board level component interfaces with another board level component at some boundary. Every electrical board description must contain the components necessary to represent the behavior of the board level component being described within its boundaries. The boundary definition depends upon the board level component being described.

For CARD EDGE CONNECTIONS such as a SIMM or a PC Daughter Card plugged into a SIMM Socket or Edge Connector, the boundary should be at the end of the board card edge pads as they emerge from the connector.

For any THROUGH-HOLE MOUNTED COMPONENT, the boundary will be at the surface of the board on which the component is mounted.

SURFACE MOUNTED COMPONENT models end at the outboard end of their recommended surface mount pads.

If the board level component contains an UNMATED CONNECTOR, the unmated connector will be described in a separate file, with its boundaries being as described above for the through-hole or surface mounted component.

Sub-Params: Len, L, R, C, Fork, Endfork, Pin, and Node. - Usage Rules: Each individual connection path (user pin to node(s)) description begins with the [Path Description] keyword and a path name, followed by the subparameters used to describe the path topology and the electrical characteristics of each section of the path. The path name must not exceed 40 characters, blanks are not allowed, and each occurrence of the [Path Description] keyword must be followed by a unique path name. Every signal pin (pins other than POWER, GND or NC) must appear in one and only one path description per [Begin Board Description]/[End Board Description] pair. Pin names do not have to appear in the same order as listed in the [Pin List] table. The individual subparameters are broken up into those that describe the electrical properties of a section, and those that describe the topology of a path.

Section Description Subparameters:

The Len, L, R, and C subparameters specify the length, the series inductance, resistance, and the capacitance to ground of each section in a path description.

Len

The physical length of a section. Lengths are given in terms of arbitrary 'units'. Any non-zero length requires that the parameters that follow must be interpreted as distributed elements by the simulator.

#51 Path Description

```
|
|  An Example Path For a SIMM Module:
|
[Path Description] CAS_2
Pin J25
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u21.15
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u22.15
Len = 0.5 L=8.35n C=3.34p R=0.01 /
Node u23.15
|
|  A Description Using The Fork and Endfork Subparameters:
|
[Path Description] PassThru1
Pin B5
Len = 0    L=2.0n /
Len = 2.1 L=6.0n C=2.0p /
  Fork
    Len = 1.0 L = 1.0n C= 2.0p /
    Node u23.15
  Endfork
Len = 1.0 L = 6.0n C=2.0p /
Pin A5
|
|  A Description Including a Discrete Series Element:
|
[Path Description] sig1
Pin B27
Len = 0    L=1.6n /
Len = 1.5 L=6.0n C=2.0p /
Node R2.1
Node R2.2
Len = 0.25 L=6.0n C=2.0p /
Node U25.6
|
```


L

The series inductance of a section, in terms of 'inductance/unit length'. For example, if the total inductance of a section is 3.0 nH and the length of the section is 2 'units', the inductance would be listed as $L = 1.5 \text{ nH}$ (i.e. $3.0 / 2$).

C

The capacitance to ground of a section, in terms of capacitance per unit length.

R

The series DC (ohmic) resistance of a section, in terms of ohms per unit length.

Topology Description Subparameters:

The Fork and Endfork subparameters denote branches from the main pin-to-node or pin-to-pin connection path. The Node subparameter is used to reference the pin of a component or board as defined in a .ibs or .ebd file. The Pin subparameter is used to indicate the point at which a path connects to a user visible pin.

Fork

This subparameter indicates that the sections following (up to the Endfork subparameter) are part of a branch off of the main connection path. This subparameter has no arguments.

Endfork

This subparameter indicates the end point of a branch. For every Fork subparameter there must be a corresponding Endfork subparameter. As with the Fork subparameter, the Endfork subparameter has no arguments. The Fork and Endfork parameters must appear on separate lines.

Node reference_designator.pin

This subparameter is used when the connection path connects to a pin of another, externally defined component. The arguments of the Node subparameter indicate the pin and reference designator of the external component. The pin and reference designator portions of the argument are separated by a period ("."). The reference designator is mapped to an external component description (another .ebd file or .ibs file) by the [Reference Designator Map] Keyword. Note that a Node MUST reference a model of a passive or active component. A Node is not an arbitrary connection point between two elements or paths.

Pin

This subparameter is used to mark the point at which a path description connects to a user accessible pin. Every path description must contain at least one occurrence of the Pin subparameter. It may also contain the reserved word NC. The value of the Pin subparameter must be one of the pin names listed in the [Pin List] section.

Note: The reserved word NC can also be used in path descriptions in a similar manner as the subparameters in order to terminate paths. This usage is optional.

Using The Subparameters to Describe Paths:

A section description begins with the Len subparameter and ends with the slash (/) character. The value of the Len, L, R, and C subparameters and the subparameter itself are separated by an equals sign (=); whitespace around the equals sign is optional. The Fork, Endfork, Node and Pin subparameters are placed between section descriptions (i.e., between the concluding slash of one section and the 'Len' parameters that starts another). The arguments of the Pin and Node subparameter is separated by white space.

Specifying a Len or L/R/C value of zero is allowed.

If Len = 0 is specified, then the L/R/C values are the total for that section. If a non-zero length is specified, then the total L/R/C for a section is calculated by multiplying the value of the Len subparameter by the value of the L, R, or C subparameter. However, as noted below, if a non-zero length is specified, that section MUST be interpreted as distributed elements.

Legal Subparameter Combinations for Section Descriptions:

- A) Len, and one or more of the L, R and C subparameters. If the Len subparameter is given as zero, then the L/R/C subparameters represent lumped elements. If the Len subparameter is non-zero, then the L/R/C subparameters represent distributed elements and both L and C must be specified, R is optional. The segment Len / must not be split; the whole segment must be on one line.
- B) The first subparameter following the [Path Description] keyword must be 'Pin', followed by one or more section descriptions. The path description can terminate in a Node, another pin or the reserved word, NC. However, NC may be optionally omitted.

Dealing With Series Elements:

A discrete series R or L component can be included in a path description by defining a section with Len=0 and the proper R or L value. A discrete series component can also be included in a path description by writing two back to back node statements that reference the same component (see the example below). Note that both ends of a discrete, two terminal component MUST be contained in a single [Path Description]. Connecting two separate [Path Description]s with a series component is not allowed.

Table 7 (cont.): Board Properties

Keyword	Syntax	Rules	Notes
[Reference Designator Map]	List of all the reference designators called by the Node subparameters in the various path descriptions. 10 characters max.	Maps a reference designator to a component or electrical board description in a .ibs or .ebd file	Note 33. Example #52
[End Board Description]		End of the electrical connect description	Example #53
[End]		End of the .ibs, .pkg or .ebd file	Example #54

Note 33

The [Reference Designator Map] keyword must be followed by a list of all of the reference designators called out by the Node subparameters used in the various path descriptions. Each reference designator is followed by the name of the .ibs or .ebd file containing the electrical description of the component or board, then the name of the component itself as given by the .ibs or .ebd file's [Component] or [Begin Board Description] keyword respectively. The reference designator, file name and component name terms are separated by whitespace. By default the .ibs or .ebd files are assumed to exist in the same directory as the calling .ebd file. It is legal for a reference designator to point to a component that is contained in the calling .ebd file.

#52 Reference Designator Map

```
[Reference Designator Map]
|
|   External Part References:
|
| Ref Des   File name   Component name
u23         pp100.ibs    Pentium(R)___Pro_Processor
u24         simm.ebd     16Meg X 36 SIMM Module
u25         ls244.ibs    National 74LS244a
u26         r10K.ibs     My_10K_Pullup
|
```

#53 End Board Description/End

```
[End Board Description]      | End: 16Meg X 8 SIMM Module
|
[End]
```

[END]